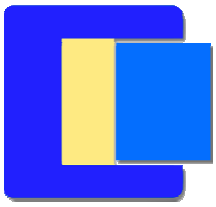


YSM343A

Data Sheet

8 Bit General Purpose OTP MCU

16-I/O with SPI, I2C, PWM and A/D

Preliminary

Revision History

1.0	Initial Version
1.1	Preliminary Version

1.0 Device Overview

1.1 General Description:

The YSM343A is a 16 I/O PIN OTP-Base 8-bit microcontroller that is high performance, low cost RISC-MCU. The Peripheral support the SPI,I2C,PWM & 6-CH 10 bits A/D Converter. The YSM343A device has eight-level deep stack, and external interrupt sources.

The YSM343A is a 16-bit wide instruction word, support the direct and indirect addressing mode.

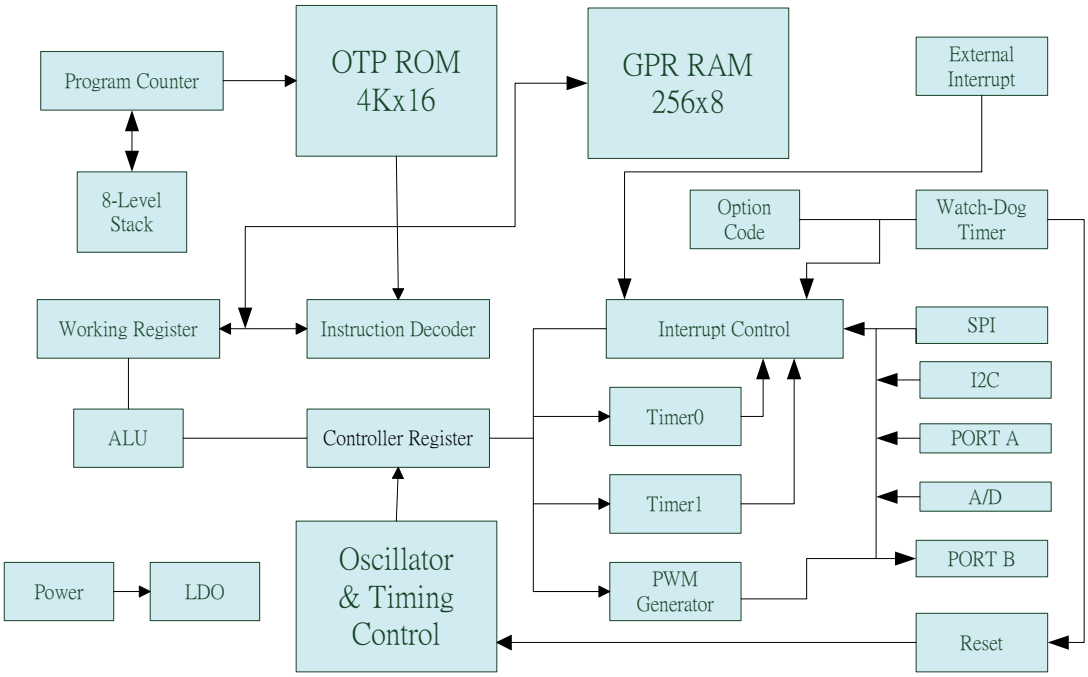
There are four oscillator options, High Speed frequency crystal mode, Low-Speed frequency crystal mode and Internal Resistor/Capacitor mode.

The sleep mode offers power saving , user can wake-up YSM343A from sleep through external , internal and Reset.

1.2 Features:

- Only 50 instructions to learn.
- All instructions are single cycle except for program branches which are two cycle.
- 16-bit wide instruction.
- 8-level deep hardware stack.
- 4K x 16-bit OTP-ROM Program Memory.
- 256 x 8-bit RAM Data Memory.
- 16 General Purpose I/O PIN.
- Built-in Internal RC oscillator.
- Two system clocks per instruction cycle.
- All I/O PIN can be Wake up.
- 2 I/O PIN with PWM Output.
- One Set SPI & I2C Interface Interrupt.
- 8-CH 10 bits A/D Converter Interrupt.
- Timer0(TCC), Timer1,Timer2,Timer3 Interrupt Source.
- 8-bit real time clock/counter
- Power On Reset, External Reset & Watch-Dog Timer Reset.
- Low Voltage Reset & Low Voltage Detect setting.
- 8 I/O Port can be selected Pull-Up/Pull-Down Resistor or Open Drain Output.

1.3 Function Block



1.4 Pin Description

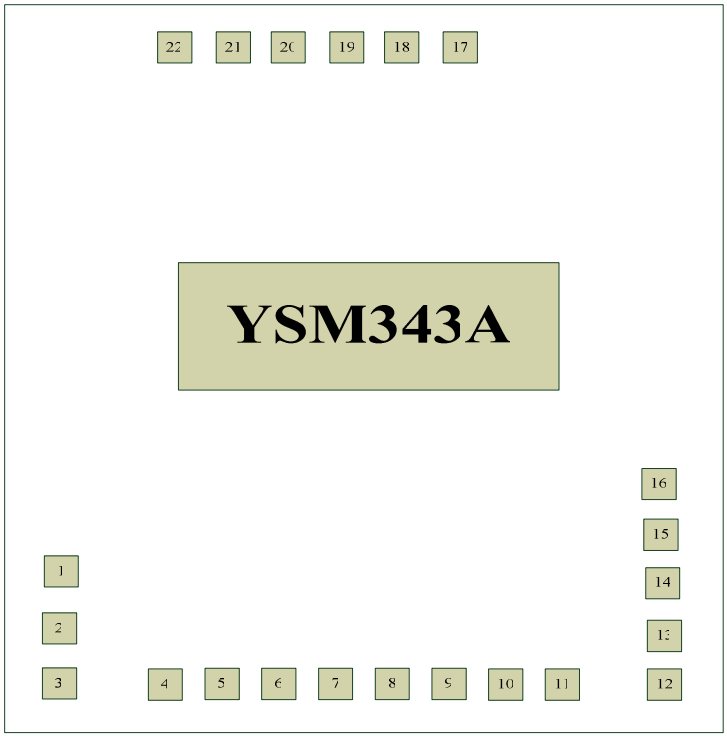
Pin Name	Pin Number	Type	Description
VDD	16	P	Power PAD, Positive Supply
VDDL	17	P	(a) System Power < 3.6V Connected with VDD. (b) System Power > 3.6V Connected with 0.1uF capacitor to VSS
VDDA	15	P	Power for Analog.
VSS	13	P	Ground PAD
VSSA	14	P	Ground for Analog
VREF	4	I	A/D Reference Voltage.
PB3 **RSTN** **(VPP)**	20	I/O I **(W)**	Pin function defined by Code-Option (a)Bi-direction I/O with pull-Hi/Low Resistor PIN Change Wake-Up after Sleep. (b)Reset Pin, Low Active, Smit-Trigger with pull-up **Write PIN**
PB0 **EINT** **SDI** **(DIO1)**	3	I/O I I **(W)**	Pin function defined by Code-Option (a)Bi-direction I/O with pull-Hi/Low Resistor PIN Change Wake-Up after Sleep. Open-Drain Output (by Software Setting) (b) EINT : Interrupt PIN (c)SDI: SPI Data In. **Write PIN**
PB5 **OSCI**	18	I/O I	Pin function defined by Code-Option (a)Bi-direction I/O with pull-Hi Resistor PIN Change Wake-Up after Sleep Open-Drain Output (by Software Setting) (b) OSCI : Xtal Mode (Oscillator Crystal Iutput) RC Mode (Connected a resistor

			to VDD)
PWM2		O	(c) PWM2 : PWM2 Output
(tCS)		**(W)**	**Write PIN**
PB4	19	I/O	Pin function defined by Code-Option (a)Bi-direction I/O with pull-Hi Resistor PIN Change Wake-Up after Sleep Open-Drain Output (by Software Setting)
OSCO		O	(b) OSCO : Xtal Mode (Oscillator Crystal output) RC Mode (Output internal system clock)
PWM1		O	(c) PWM1 : PWM1 Output.
CKO		O	(d) Clock Out Setting By Option
(tSCK)		**(W)**	**Write PIN**
PB1	2	I/O	Pin function defined by Code-Option (a)Bi-direction I/O with pull-Hi/Low Resistor PIN Change Wake-Up after Sleep Open-Drain Output (by Software Setting)
SDO		O	(b) SDO:SPI Data Output
PWM1		O	(c) PWM1:PWM1 Output.
(DIO2)		**(W)**	**Write PIN**
PB2	1	I/O	Pin function defined by Code-Option (a)Bi-direction I/O with pull-Hi/Low Resistor PIN Change Wake-Up after Sleep Open-Drain Output (by Software Setting)
TCC		I	(b) TCC: External Clock/Counter Input.
SCK		I/O	(c) SCK: SPI Clock In.
PWM2		O	(d) PWM2: PWM2 Output.
PB6	21	I/O	Pin function defined by Code-Option (a)Bi-direction I/O with pull-Hi Resistor PIN Change Wake-Up after Sleep Open-Drain Output (by Software Setting)
SSB		I	(b) SSB : SPI Slave Selected PIN.

PWM1 **SCL** **CKO**		O I/O O	(c) PWM1: PWM1 Output. (d) I2C-SCL PIN (e) Clock Out Setting By SFR ***IOFS***
PB7 **PWM2** **SDA**	22	I/O O I/O	Pin function defined by Code-Option (a)Bi-direction I/O with pull-Hi Resistor PIN Change Wake-Up after Sleep Open-Drain Output (by Software Setting) (b) PWM2 : PWM2 Output (c) I2C-SDA PIN
PA0 **SDI** **AD0**	5	I/O I I	(a) Bi-direction I/O with pull-Low Resistor (b) SDI : SPI Data In. (c) Analog IN for A/D Converter Channel 0.
PA1 **SCK** **AD1**	6	I/O I/O I	(a) Bi-direction I/O with pull-Low Resistor (b) SCK: SPI Clock In. (c) Analog IN for A/D Converter Channel 1.
PA2 **AD2**	7	I/O I	(a) Bi-direction I/O with pull-Low Resistor (b) Analog IN for A/D Converter Channel 2.
PA3 **AD3**	8	I/O I	(a) Bi-direction I/O with pull-Low Resistor (b) Analog IN for A/D Converter Channel 3.
PA4 **AD4**	9	I/O I	(a)Bi-direction I/O with pull-Hi/Low Resistor (b) Analog IN for A/D Converter Channel 4.
PA5 **AD5**	10	I/O I	(a) Bi-direction I/O with pull-Hi/Low Resistor (b) Analog IN for A/D Converter Channel 5.
PA6 **AD6**	11	I/O	(a) Bi-direction I/O with pull-Hi/Low Resistor (b) Analog IN for A/D Converter Channel 6.

SCL			(c) I2C Clock PIN
PA7 **AD7** **SDA**	12	I/O	Bi-direction I/O with pull-Hi/Low Resistor (b) Analog IN for A/D Converter Channel 7. (c) I2C Data PIN

1.5 Pad Location :



NO.	PAD NAME	X	Y		NO.	PAD NAME	X	Y
1	PB2	-511	-572		12	PA7	511	-755
2	PB1	-511	-662		13	VSS	511	-665
3	PB0/EINT	-511	-752		14	VSSA	511	-575
4	VREF	-307	-759		15	VDDA	512	-485
5	PA0	-217	-759		16	VDD	512	-395
6	PA1	-127	-759		17	VDDL	116	759
7	PA2	-37	-759		18	PB5	26	759
8	PA3	52	-759		19	PB4	-63	759
9	PA4	142	-759		20	PB3/RSTN	-153	759
10	PA5	232	-759		21	PB6	-243	759
11	PA6	322	-759		22	PB7	-333	759

Table of Contents

2.0 Memory Organization

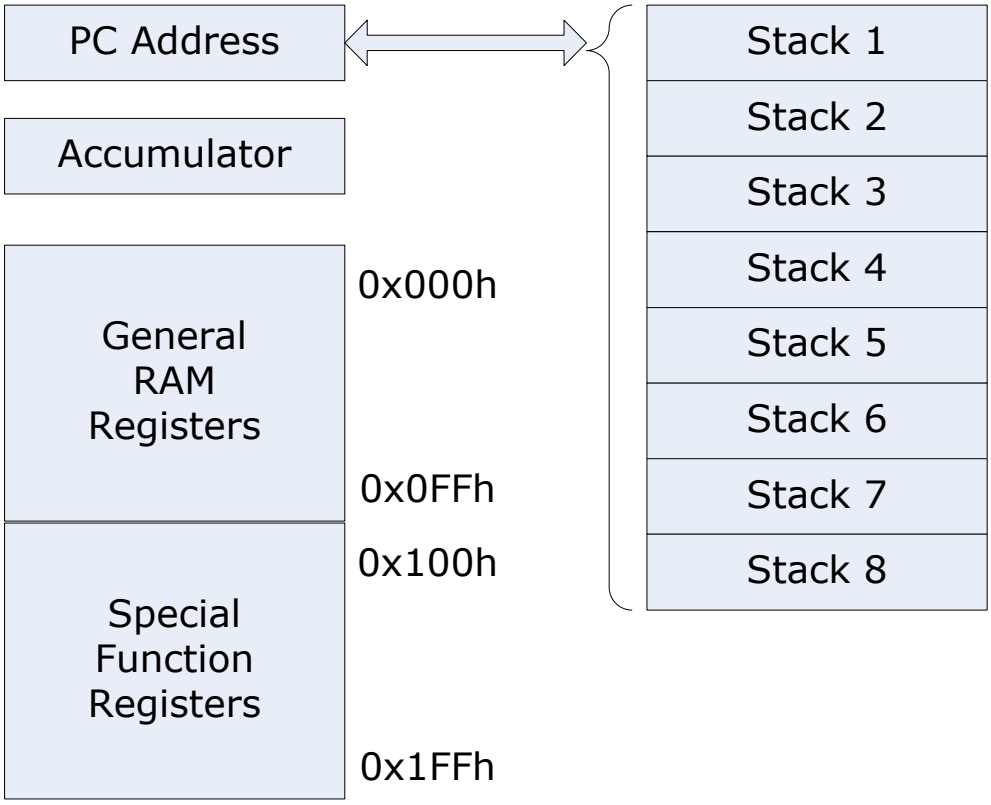
2.1 ROM Structure

Address	***Description***
0x0000	**Reset Vector** Power-On , RSTN PIN go low
0x0003	**LVD Interrupt Vector** LVD(Low Voltage Detect) Interrupt
0x0005	**External Interrupt Vector** EINT PIN Interrupt
0x0007	**PIN Change Interrupt Vector** I/O PIN Input PIN Change Wake-Up Interrupt
0x0009	**TCC Overflow Interrupt Vector** TCC(Timer0) Overflow Interrupt
0x000B	**WDT Interrupt Vector** WDT(Watch Dog Timer) Timer Out Interrupt
0x000D	**ADC Interrupt Vector** 8-Channel A/D Interrupt
0x0011	**Timer1 Interrupt Vector** Timer1 Interrupt
0x0013	**Timer2 Interrupt Vector** Timer2 Interrupt
0x0015	**Timer3 Interrupt Vector** Timer3 Interrupt
0x0017	**SPI Interrupt Vector** SPI Interrupt
0x001B	**I2C Interrupt Vector** I2C Interrupt
0x001C ~0x0020	**Interrupt Vector Reserve**
0x0003 ~0x0FFF	**Program Area** General coding area.

(Continue)

Address	*Description*
N/A	**Option Codes** The ROM space which used to store the device options.

2.2 RAM Structure



There are 256 bytes general purpose registers(GPRs) in RAM of the MCU, User can use these GPRs by direct addressing without any page/bank change commands.

The 2nd block of the RAM space are the Special Function Registers(SFRs). These are being accessed like GPRs by direct addressing.

Notes. GPRs/SFRs can only move the value to/from the accumulator.

2.3 RAM – Special Function Registers(SFRs) Overview

YSM343 Special Function Registers									
NAME	**ADDR**	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
INDR	0x100	**Indirect Addressing Register**							
TMR0	0x101	**8 bit Real Time Clock / Counter**							
PCL	0x102	**Low 8 bits Program Counter Register**							
STATUS	0x103	GPR	-	-	/TO	/PD	Z	DC	C
RAMS	0x104	**Indirect Data Memory Address Point**							
PORTA	0x105	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
PORTB	0x106	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
PAS	0x115	PAS7	PAS6	PAS5	PAS4	PAS3	PAS2	PAS1	PAS0
PBS	0x116	PBS7	PBS6	PBS5	PBS4	PBS3	PBS2	PBS1	PBS0
PBW	0x120	WB7	WB6	WB5	WB4	WB3	WB2	WB1	WB0
PAW	0x121	WA7	WA6	WA5	WA4	WA3	WA2	WA1	WA0
MCR	0x122	T0CS1	GIE	T0CS0	TM0CE	PAB	PS2	PS1	PS0
ODB	0x123	ODB7	ODB6	ODB5	ODB4	-	ODB2	ODB1	ODB0
IORA	0x125	IOA7	IOA6	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0
IORB	0x126	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0
IOPA	0x12A	/PUA7	/PUA6	/PUA5	/PUA4	/PDA7	/PDA6	/PDA5	/PDA4
IOPD	0x12B	/PDB3	/PDB2	/PDB1	/PDB0	/PDA3	/PDA2	/PDA1	/PDA0
T1CON	0x12C	-	-	-	-	-	TR1S	TR1P1	TR1P0
IOPH	0x12D	/PUB7	/PUB6	PUB5	/PUB4	/PUB3	/PUB2	/PUB1	/PUB0
WDTS	0x12E	EIS	EIT	WDTE	SLP2E	WDCKS			
INTE	0x12F	WDTIE	-	-	ICIE	TR1IE	SPIIE	EXIE	TR0IE
PWM1D	0x130	**PWM1 Duty Cycle Data Register**							
PWM2D	0x131	**PWM2 Duty Cycle Data Register**							
PWM1P	0x132	**PWM1 Period Data Register**							
PWM2P	0X133	**PWM2 Period Data Register**							
PWMC	0x134	PW2E	PW1E	P2S2	P2S1	P2S0	P1S2	P1S1	P1S0
T23CON	0x135	TR2S	TR2IE	TR2IF	TR3S	TR3IE	TR3IF	POINV	T23CS
SPIRB	0x13A	**SPI Data Read Buffer**							
SPIWB	0x13B	**SPI Data Write Buffer**							
SPIS	0x13C	**SPI Status Register**							
SPIC	0x13D	CES	SPIE	SRO	SSE	ORD	SBRS2	SBRS1	SBRS0

YSM343 Special Function Registers(Continue)									
NAME	**ADDR**	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
TMR1	0x13E	**Timer1 Value Register**							
TR1CV	0x13F	**Timer 1 Comparator Value Register**							
ADCON1	0x140	ADC	ADEN	ADIE	ADIF	CHS3	CHS2	CHS1	CHS0
ADLSB	0x141	AD01	AD00	-	-	-	-	-	-
ADMSB	0x142	AD09	AD08	AD07	AD06	AD05	AD04	AD03	AD02
ADCON2	0x343	SHE	VREFS	-	-	-	ADCS2	ADCS1	ADCS0
I2CCON	0x144	I2CE	RSTA	SSBG	MSM	ACKTX	RW	BUSY	ARBL
I2CSTA	0x145	I2RIE	I2RIF	I2TIE	I2TIF	STIE	STIF	-	-
I2CDAT	0x146	I2CD7	I2CD6	I2CD5	I2CD4	I2CD3	I2CD2	I2CD1	I2CD0
I2CADR	0x147	I2CA6	I2CA5	I2CA4	I2CA3	I2CA2	I2CA1	I2CA0	-
PAL	0x14B	**Low- Byte Address of Data Latch**							
PAH	0x14C	**High-Byte Address of Data Latch**							
IOSK2	0x171	-	-	-	-	-	-	-	PBHS
IOFS	0x172	I2CP1	I2CP0	0	CKO1	CKO0	SPIOS	PMS1	PMS0
IOBUF2	0x173	-	-	-	-	-	-	-	PBHT
IOSK1	0x174	PA23S	PA01S	PB7S	PB6S	PB45S	PB23S	PB1S	PB0S
IOBUF1	0x175	PA23T	PA01T	PB7T	PB6T	PB45T	PB23T	PB1T	PB0T
IOTPS	0x17A	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0
LDOC	0x17B	LDOS	LDWE	LDSE	LDOP	-	-	-	-
GCKC	0x17C	GSYS	GIO	GTR1	GEIN	-	GSPI	-	GPWM
LVRC	0x17D	LVRE	LVDIF	LVDIE	LVFC1	LVFC0	LVS2	LVS1	LVS0
INTF	0x17F	WDTIF	-	-	ICIF	TR1IF	SPIIF	EXIF	TR0IF

2.4 Special Function Registers(SFRs) Briefing

◆ **INDR** (0x100) : ***Indirect Addressing Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INDR	Indirect Addressing Register							
R/W	R/W							
RESET	-	-	-	-	-	-	-	-

The INDR Register is not a physical register. Addressing INDR actually address the register that RAMS address value. User should use SFR:INDR with SFR:RAMS to access the indirect addressing data.

◆ **TMR0** (0x101) : ***8Bits Real Timer Clock/Counter***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TMR0	8 bit Real Time Clock / Counter							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

The TMR0 special function register is the clock counter value which the clock source is from an 8bits real time clock. And the clock source of the 8bits real time clock is from the instruction cycle(Fosc / 2) or TCC pin or OSCO clock.

◆ **PCL** (0x102) : ***Program Counter Lower 8 bits data***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PCL	Low 8 bits Program Counter Register							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET								

The PCL special function register is the lower 8 bits data of the program counter.

◆ **STATUS** (0x103) : ***Status Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STATUS	GPR	-	-	/TO	/PD	Z	DC	C
R/W	R/W	-	-	R/W	R/W	R/W	R/W	R/W
RESET	0	-	-	1	1	0	0	0

GPR : ***General Purpose Read/Write bit***

/TO : ***Time- Out Flag***

/TO=0 Watch dog Timer Overflow.

/TO=1 (a) Power On

(b) Execute WDTC or SLEEP Instruction.

/PD : ***Power Down Flag***

/PD=0 After SLEEP Instruction.

/PD=1 (a) Power On

(b) Execute WDTC Instruction.

Z : ***ALU Operation Zero Flag***

Z=0 Operation Result is not Zero.

Z=1 Operation Result is Zero.

DC : ***ALU Operation Half Carry /Borrow Flag***

DC=0 Half Carry/Borrow does not occur.

DC=1 Half Carry/Borrow occurred.

C : ***ALU Operation Carry /Borrow Flag***

C=0 Carry/Borrow does not occur.

C=1 Carry/Borrow occurred.

◆ **RAMS** (0x104) : ***Indirect Addressing Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RAMS	Indirect Data Memory Address Point							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET								

The RAMS register is a pointer for Indirect Addressing . User should use SFR:INDR with SFR:RAMS to access the indirect addressing data.

◆ **PORTA** (0x105) : ***Port A Data***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PORTA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

PA0~PA7 : *I/O Port Output Data*

◆ **PORTB** (0x106) : ***Port B Data***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PORTB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

PB0~PB7 : *I/O Port Output Data*

◆ **PAS** (0x115) : ***Port A Pin Status Data***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PAS	PAS7	PAS6	PAS5	PAS4	PAS3	PAS2	PAS1	PAS0
R/W	R	R	R	R	R	R	R	R
RESET	-	-	-	-	-	-	-	-

PAS0~PAS7 : *I/O Port Reading Data From Pin Status.*

◆ **PBS** (0x116) : ***Port B Pin Status Data***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PBS	PBS7	PBS6	PBS5	PBS4	PBS3	PBS2	PBS1	PBS0
R/W	R	R	R	R	R	R	R	R
RESET	-	-	-	-	-	-	-	-

PBS0~PBS7 : *I/O Port Reading Data From Pin Status.*

◆ **PBW** (0x120) : ***Port B Wake Up Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PBW	WB7	WB6	WB5	WB4	WB3	WB2	WB1	WB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET								

WB7~0 : *Port B PIN Wake Up Enable*

WB7~0=1 , Port B7~B0 can be wake –up

Wake Up Condition : As a Input Port & Input Signal from High to Low / Low to High.

WB7~0=0 , Disable.

I/O Port as a Wake Up PIN Setting Procedure:

Step 1: Setting as a Input PIN

Step 2: Pull Up/ Pull Down Enable .

Step 3: Enable Wake Up Function

Step 4: Enter to Sleep.

◆ **PAW** (0x121) : ***Port A Wake Up Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PAW	WA7	WA6	WA5	WA4	WA3	WA2	WA1	WA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET								

WA7~0 : *Port A PIN Wake Up Enable*

WA7~0=1 , Port A7~A0 can be wake –up

Wake Up Condition : As a Input Port & Input Signal from High to Low / Low to High.

WA7~0=0 , Disable.

◆ **MCR** (0x122) : ***Main Control Register for Read / Write***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MCR	T0CS1	GIE	T0CS0	TM0CE	PAB	PS2	PS1	PS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET								

GIE : ***Global Interrupt Enable.***

GIE=0 Disable all interrupts. Execute DISI Instruction or accept Interrupt then GIE will be set to '0'. Reject any other Interrupt.

GIE=1 Global Enable all the Interrupt (Enable or not depend on others Register Enable Bit.
Execute ENI or RETI will be set to '1'. then accept others Interrupt.

T0CS1~T0CS0 : ***Timer-0 Clock Source .***

T0CS1	T0CS0	Timer 0 Clock Source
1	1	Instruction cycle(Fosc/2)
1	0	External TCC clock (PB2)
0	1	OSCO clock
0	0	Reserved

TM0CE : ***Timer-0 Counting edge while using external TCC.***

TM0CE=0 Timer-0 increasing at TCC rising edge.

TM0CE=1 Timer-0 increasing at TCC falling edge.

PAB : ***Prescaler bit Assignment .***

PAB=0 Assign to TMR0 (Timer 0).

PAB=1 Assign to WDT (Watch-Dog Timer).

(Continue)

PS2~PS0 : ***Prescaler bits.***

PS2	PS1	PS0	TMR0 Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

◆ **ODB** (0x123) : ***Port B Open-Drain Setting***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ODB	ODB7	ODB6	ODB5	ODB4	-	ODB2	ODB1	ODB0
R/W	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
RESET								

ODB7~ODB0 : *Each Port B Open-Drain Enable Bit*

ODB7~0=1 , Open Drain Enable.

ODB7~0=0 , Open Drain Disable.

◆ **IORA** (0x125) : ***Port A I/O Direction Setting***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IORA	IOA7	IOA6	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

◆ **IORB** (0x126) : ***Port B I/O Direction Setting***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IORB	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

IOx0~IOx7 : *I/O as a Input or Output*

IOx0~7=0 , as a Output.

IOx0~7=1 , as a Input.

Port B can be Wake Up (from High to Low) after Sleep if (/WUE)=0.

◆ **IOPA** (0x12A) : ***Port A I/O Pull Resistor Setting***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IOPA	/PUA7	/PUA6	/PUA5	/PUA4	/PDA7	/PDA6	/PDA5	/PDA4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

/PUAx : *I/O pins Pull-high resistor*

/PUAx=0 , Enable the pull-high resistor(PortA7~4).

/PUAx=1 , Disable the pull-high resistor(PortA7~4).

/PDAx : *I/O pins Pull-low resistor*

/PDAx=0 , Enable the pull-down resistor(PortA7~4).

/PDAx=1 , Disable the pull-down resistor(PortA7~4).

◆ **IOPD** (0x12B) : ***I/O Port Pull Down Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IOPD	/PDB3	/PDB2	/PDB1	/PDB0	/PDA3	/PDA2	/PDA1	/PDA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

/PDA3~/PDA0 : ***Each I/O Port Pull-Down Enable Bit***

/PDAx=0 , Enable the pull-down resistor(PortA3~0).

/PDAx=1 , Disable the pull-down resistor(PortA3~0).

/PDB3~/PDB0 : ***Each I/O Port Pull-Down Enable Bit***

/PDBx=0 , Enable the pull-down resistor(PortB3~0).

/PDBx=1 , Disable the pull-down resistor(PortB3~0).

◆ **T1CON** (0x12C) : ***Timer 1 Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
T1CON	-	-	-	-	-	TR1S	TR1P1	TR1P0
R/W	-	-	-	-	-	R/W	R/W	R/W
RESET	-	-	-	-	-	0	0	0

TR1S : ***Timer 1 Turn On Bit***

TR1S=0 , Timer 1 turn off.

TR1S=1 , Timer 1 turn on.

TR1P1,TR1P0 : ***Timer 1 Prescaler Rate***

TR1P1	TR1P0	TMR0 Rate
0	0	1:1
0	1	1:4
1	0	1:8
1	1	1:16

◆ **IOPH** (0x12D) : ***I/O Port Pull High Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IOPH	/PUB7	/PUB6	PUB5	/PUB4	/PUB3	/PUB2	/PUB1	/PUB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

/PUB7~/PUB0 : ***Each I/O Port Pull-Up Enable Bit***

/PUB7~/PUB0=0 , Enable (Connected with Pull High Resistor).

/PUB7~/PUB0=1 , Disable(disconnect with Pull High Resistor).

◆ **WDTS** (0x12E) : ***Watch Dog & Wake Up Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WDTS	EIS	EIT	WDTE	SLP2E	WDCKS	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	-	-	-
RESET	0	0	1	1	0	-	-	-

EIS : ***External Interrupt PIN Selection***

EIS=0 , PB0 is as a GPIO PIN.

EIS=1 , PB0 is as a EINT (External Interrupt PIN).

EIT : ***External Interrupt Type***

EIT=0 ,External Interrupt on falling edge.

EIT=1 ,External Interrupt on rising edge.

WDTE : ***Watch Dog Timer Enable***

WDTE=1 ,Watch Dog Timer Enable When Option Selection Bit (ENWDT =1) .

WDTE=0 , Disable.

SLP2E : ***Sleep2 Mode Control Bit***

SLP2E=0 , Enter the Sleep2 Mode Status.

SLP2E=1 ,Otherwise.

WDCKS : ***Watch Dog Clock Source Selecctionr***

WDCKS=0 , Internal RC-Oscillator (around 14Khz).

WDCKS=1 , Clock Source is from OSCO(System Clock =Internal RC Oscillator).

◆ **INTE** (0x12F) : ***Hardware Interrupt Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTE	WDTIE	-	-	ICIE	TR1IE	SPIIE	EXIE	TR0IE
R/W	R/W	-	-	R/W	R/W	R/W	R/W	R/W
RESET	0	-	-	0	0	0	0	0

TR0IE : *Timer 0 Interrupt Enable*

TR0IE=0 , Timer 0 Interrupt Disable .

TR0IE=1 , Timer 0 Interrupt Enable .

EXIE : *External Interrupt Enable*

EXIE=0 , External Interrupt Disable .

EXIE=1 , External Interrupt Enable .

SPIIE : *SPI Interrupt Enable*

SPIIE=0 , SPI Interrupt Disable .

SPIIE=1 , SPI Interrupt Enable .

TR1IE : *Timer 1 Interrupt Enable*

TR1IE=0 , Timer 1 Interrupt Disable .

TR1IE=1 , Timer 1 Interrupt Enable .

ICIE : *I/O port Change Interrupt Enable*

ICIE=0 , I/O Port-Change Interrupt Disable .

ICIE=1 , I/O Port-Change Interrupt Enable .

WDTIE : *Watch Dog Timer Time-Out Interrupt Enable*

WDTIE=0 , WDT Time-Out Interrupt Disable .

WDTIE=1 , WDT Time-Out Interrupt Enable .

◆ **PWM1D** (0x130) : ***PWM1 Duty Cycle Data Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM1D	P1D7	P1D6	P1D5	P1D4	P1D3	P1D2	P1D1	P1D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

◆ **PWM2D** (0x131) : ***PWM2 Duty Cycle Data Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM2D	P2D7	P2D6	P2D5	P2D4	P2D3	P2D2	P2D1	P2D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

P1D7~P1D0 : ***8 bits PWM1 Duty Cycle Data***

P2D7~P2D0 : ***8 bits PWM2 Duty Cycle Data***

◆ **PWM1P** (0x132) : ***PWM1 Period Data Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM1P	P1P7	P1P6	P1P5	P1P4	P1P3	P1P2	P1P1	P1P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

◆ **PWM2P** (0x133) : ***PWM2 Period Data Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM2P	P2P7	P2P6	P2P5	P2P4	P2P3	P2P2	P2P1	P2P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

P1P7~P1P0 : ***8 bits PWM1 Period Data , PWM1 Signal Output from PB1 PIN.***

P2P7~P2P0 : ***8 bits PWM2 Period Data , PWM2 Signal Output from PB2 PIN.***

◆ **PWMC** (0x134) : ***PWM Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWMC	PW2E	PW1E	P2S2	P2S1	P2S0	P1S2	P1S1	P1S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

PW2E : ***PWM2 Enable Bit***

PW2E=0 , PWM2 Disable.

PW2E=1 , PWM2 Enable.

PW1E : ***PW12 Enable Bit***

PW1E=0 , PWM1 Disable.

PW1E=1 , PWM1 Enable.

PxS2,PxS1,PxS0 : PWM Clock Prescaler ***Rate(x=1 or 2)***

PxS2	PxS1	PxS0	PWM Clock Rate
0	0	0	Fosc/2
0	0	1	Fosc/4
0	1	0	Fosc/8
0	1	1	Fosc/16
1	0	0	Fosc/32
1	0	1	Fosc/64
1	1	0	Fosc/128
1	1	1	Fosc/256

◆ **T23CON** (0x135) : ***Timer Setting and PWM Setting Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
T23CON	TR2S	TR2IE	TR2IF	TR3S	TR3IE	TR3IF	POINV	T23CS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

TR2S : *Timer 2 Enable*

TR2S=0 , Timer 2 Disable.

TR2S=1 , Timer 2 Enable.

TR2IE : *Timer 2 Interrupt Enable*

TR2IE=0 , Timer 2 Interrupt Disable.

TR2IE=1 , Timer 2 Enable.

TR2IF : *Timer 2 Interrupt Flag*

TR2IF=0 , Clear by software.

TR2IF=1 , Timer 2 interrupt occurred.

TR3S : *Timer 3 Enable*

TR3S=0 , Timer 3 Disable.

TR3S=1 , Timer 3 Enable.

TR3IE : *Timer 3 Interrupt Enable*

TR3IE=0 , Timer 3 Interrupt Disable.

TR3IE=1 , Timer 3 Enable.

TR3IF : *Timer 3 Interrupt Flag*

TR3IF=0 , Clear by software.

TR3IF=1 , Timer 3 interrupt occurred.

POINV : *PWM output invert*

POINV=0 , Initial with low level, high level PWM pulse.

POINV=1 , Initial with high level, low level PWM pulse.

T23CS : *Timer2 and Timer3 cascade mode*

T23CS=0 , Timer2 and Timer3 standalone mode.

T23CS=1 , Timer2 and Timer3 cascaded.

◆ **SPIRB**(0X13A) : ***SPI Data Read Buffer***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIRB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R/W-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

◆ **SPIWB**(0X13B) : ***SPI Data Write Buffer***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIWB	WB7	WB6	WB5	WB4	WB3	WB2	WB1	WB0
R/W-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

SPIRB Register is a 8 bits Data Buffer for SPI Data Read In.
SPIWB Register is a 8 bits Data Buffer for SPI Data Write Out.

◆ **SPIS**(0X13C) : ***SPI Status Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIS	-	-	-	-	ODO	ODC	RBFIF	RBF
R/W-	-	-	-	-	R/W	R/W	R/W	R/W
RESET	-	-	-	-	0	0	0	0

ODO : *SDO Open-Drain Control*

ODO=0 ,SDO Open-Drain Disable.
ODO=1 ,SDO Open-Drain Enable.

ODC : *SCK Open-Drain Control*

ODC=0 ,SCK Open-Drain Disable.
ODC=1 ,SCK Open-Drain Enable.

RBFIF : *SPI Read Buffer Full Interrupt Flag*

RBFIF=1 ,(a)Receive Completed, and Read Buffer is Full.
(b) Under the Interrupt Enable, and Interrupt Occur.
RBFIF=0 ,Receive Status is Ongoing , Read Buffer is Empty.

RBFIF : *SPI Read Buffer Full Flag*

RBF=1 ,Receive Completed, and Read Buffer is Full.
RBF=0 ,Receive Status is Ongoing , Read Buffer is Empty.

◆ **SPIC**(0X13D) : ***SPI Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIC	CES	SPIE	SRO	SSE	ORD	SBRS2	SBRS1	SBRS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	-	0	0	0	0

CES : *SPI Clock Edge Selection*

CES=0 , **Low go High** , Data Out; **High go Low** Data In.

CES=1 , **High go Low** , Data Out; **Low go High** Data In.

SPIE : *SPI Enable*

SPIE=0 ,SPI Disable.

SPIE=1 ,SPI Enable.

SRO : *Data In Overflow Flag (Only Used SLAVE Mode)*

SRO=1 ,Last Byte Data in SPI Read Buffer had not Read Out .

SRO=0 ,Otherwise.

SSE : *Start Shift SPI Data Out*

SSE=1 ,(a)Start Shift SPI Data Out.

(b) Completed Working , Clear SSE bit by Hardware .

SRO=0 ,Otherwise.

ORD : *SPI Data Shift Order*

ORD=0 ,MSB Bit First.

ORD=1 ,LSB Bit First.

SBRS2~SBRS0 : *SPI Baud Rate & Mode Selection*

SBRS~SBRS0 : ***Selection bits for Baud Rate & Mode***

SBRS	SBRS1	SBRS0	Mode	Baud Rate
0	0	0	Master	Fosc/2
0	0	1	Master	Fosc/4
0	1	0	Master	Fosc/8
0	1	1	Master	Fosc/16
1	0	0	Master	Fosc/32
1	0	1	Slave	SS Enable
1	1	0	Slave	SS Disable
1	1	1	Master	TMR1/2

◆ **TMR1** (0x13E) : ***Timer 1 Value Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TMR1	Timer 1 Value Register							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

◆ **TR1CV** (0x13F) : ***Timer 1 Comparator Value Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TR1CV	Timer 1 Comparator Value Register							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

◆ **ADCON1**(0X140) : ***A/D Control Register #1***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADCON1	ADC	ADEN	ADIE	ADIF	CHS3	CHS2	CHS1	CHS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

ADC : ***ADC Start Transfer & Completed Flag***

ADC=0 , ADC is be Transfer Completed.(Clear by MCU Hardware)

ADC=1 , ADC Start Transfer.

ADEN : ***ADC Converter Enable***

ADEN=0 , ADC Converter Disable.

ADEN=1 , ADC Converter Enable.

CHS3~CHS0 : ***ADC Channel Selection***

CHS3~CHS0 = Channel 15~0.

Channel 15~8 Reserve .

◆ **ADLSB**(0X141) : ***A/D Digital Data LSB 2bits of 10bits***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADLSB	AD01	AD00	-	-	-	-	-	-
R/W	R/W	R/W	-	-	-	-	-	-
RESET	0	0	-	-	-	-	-	-

AD01~AD00 : ***ADC Transfer to Digital Data bit1~bit0***

◆ **ADMSB**(0X142) : ***A/D Digital Data MSB 8bits of 10bits***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADMSB	AD09	AD08	AD07	AD06	AD05	AD04	AD03	AD02
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

AD09~AD02 : ***ADC Transfer to Digital Data bit9~bit2***

◆ **ADCON2**(0X143) : ***A/D Control Register #2***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADCON2	SHE	VREFS	-	-	-	ADCS2	ADCS1	ADCS0
R/W	R/W	R/W	-	-	-	R/W	R/W	R/W
RESET	0	0	-	-	-	0	0	0

SHE : ***ADC Sampling & Hold Enable***

SHE=0 , ADC Sampling & Hold is Disable.

SHE=1 , ADC Sampling & Hold is Enable.

ADCS2~ADCS0 : ***ADC CLK Source:***

ADCS2	ADCS1	ADCS0	Clock (Hz)
0	0	0	Fosc/4
0	0	1	Fosc/8
0	1	0	Fosc/12
0	1	1	Fosc/16
1	0	0	Fosc/20
1	0	1	Fosc/24
1	1	0	Fosc/28
1	1	1	Fosc/32

◆ **I2CCON**(0X144) : ***I2C Protocol control register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
I2CCON	I2CE	RSTA	SSBG	MSM	ACKTX	RW	BUSY	ARBL
R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W
RESET	0	0	0	0	0	0	0	1

I2CE : ***I2C Protocol Enable***

I2CE=0 , I2C Protocol Disable.

I2CE=1 , I2C Protocol Enable.

RSTA : ***I2C Protocol Re-Start Bit Send (Master Mode)***

RSTA=0 → 1, Generate I2C protocol "Re-Start" bit.

SSBG : ***I2C Protocol Generate Start/Stop bit (Master Mode)***

SSBG=0 → 1, Generate I2C protocol "Start" bit.

SSBG=1 → 0, Generate I2C protocol "Stop" bit.

MSM : ***I2C Protocol Master/Slave Mode***

MSM=0 , I2C Protocol Slave Mode.

MSM=1 , I2C Protocol Master Mode.

ACKTX : ***I2C ACK signal sending***

When level changed, an ACK signal will be sent to SDA by clock pulse on SCL.

RW : ***I2C Protocol RW bit in header byte***

RW=0 , Transmitter on Master, Receiver on Slave.

RW=1 , Transmitter on Slave, Receiver on Master.

BUSY : ***I2C bus status***

The bit will be set to 1 if "START" signal being detected, and clear to 0 if "STOP" signal being detected.

ARBL : ***I2C arbitration lost***

The bit will be set to 1 if the bus arbitration is lost , and cleared by software.

◆ **I2CSTA**(0X145) : ***I2C Protocol status register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
I2CSTA	I2RIE	I2RIF	I2TIE	I2TIF	STIE	STIF	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
RESET	0	0	0	0	0	0	-	-

I2RIE : ***I2C Protocol Receive Interrupt enable bit***

I2RIE=0 , I2C Protocol receive interrupt disable.

I2RIE=1 , I2C Protocol receive interrupt enable.

I2RIF : ***I2C Protocol Byte Receive Flag***

I2RIF=0 , Clear by software.

I2RIF=1 , I2C Protocol had received a byte data.

I2TIE : ***I2C Protocol Transmit Interrupt enable bit***

I2TIE=0 , I2C Protocol transmit interrupt disable.

I2TIE=1 , I2C Protocol transmit interrupt enable.

I2TIF : ***I2C Protocol Byte Transmitted Flag***

I2RIF=0 , Clear by software.

I2RIF=1 , I2C Protocol had transmitted a byte data and received the ACK/nACK signal.

STIE : ***I2C Protocol Stop Bit Received Interrupt enable bit***

STIE=0 , I2C Protocol stop bit received interrupt disable.

STIE=1 , I2C Protocol stop bit received interrupt enable.

STIF : ***I2C Protocol Stop Bit Receive Flag***

STIF=0 , Clear by software.

STIF=1 , I2C Protocol had received a “STOP” bit signal.

◆ **I2CDAT**(0X146) : ***I2C Protocol Data Store register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
I2CDAT	I2CD7	I2CD6	I2CD5	I2CD4	I2CD3	I2CD2	I2CD1	I2CD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

I2CDAT register is the buffer to store the transmit/received data.

◆ **I2CSAD**(0X147) : ***I2C Slave Address Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
I2CSAD	I2CA6	I2CA5	I2CA4	I2CA3	I2CA2	I2CA1	I2CA0	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
RESET	0	0	0	0	0	0	0	-

I2CA6~0 : *I2C Protocol address (Slave Mode)*

I2CA6~0 : *I2C Protocol SCL clock rate seed(Master Mode)*

SCL Clock Rate = Fosc / (I2CA + 3) x 2

Notes: I2CA cannot be zero while as clock rate seed.

◆ **PAL** (0x14B) : ***Low Byte Address of The Data Latching***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PAL	Data Latching Address Low Byte Part							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET								

◆ **PAH** (0x14C) : ***High Byte Address of The Data Latching***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PAH	Data Latching Address High Byte Part							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET								

◆ **IOSK2**(0X171) : ***I/O Sink Enhance Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IOSK2	-	-	-	-	-	-	-	PBHS
R/W	-	-	-	-	-	-	-	R/W
RESET	-	-	-	-	-	-	-	0

PBHS : ***PortA7~4 Sink Enhancer enable***

PBHS = 0 : Disable output sink Enhancer.

PBHS = 1 : Enable output sink Enhancer.

◆ **IOFS**(0X172) : ***I/O Function Setting Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IOFS	I2CP1	I2CP0	0	CKO1	CKO0	SPIOS	PMS1	PMS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

I2CP1~0 : ***I2C port setting***

I2CP1	I2CP0	Setting
0	0	SCL=PB6 / SDA=PB7
0	1	Reserved
1	0	SCL=PA6 / SDA=PA7
1	1	Reserved

Bit5: ***Fix value, Please set to 0.***

CKO1~0 : ***Clock out from PB6***

CKO1	CKO0	Setting
0	0	No clock out
0	1	Clock out frequency = Fosc
1	0	Clock out frequency = Fosc / 2
1	1	Clock out frequency = Fosc / 4

SPIOS : ***SPI SCK/SDI port selection***

SPIOS = 0 : SCK = PB2 / SDI = PB0.

SPIOS = 1 : SCK = PA1 / SDI = PA0.

PMS1~0 : *PWM port selection*

PMS1	PMS0	Setting
0	0	PWM1 = PB1 / PWM2 = PB2
0	1	PWM1 = PB4 / PWM2 = PB5
1	0	PWM1 = PB6 / PWM2 = PB7
1	1	Reserved

◆ **IOBUF2**(0X173) : ***I/O Buffer Setting Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IOBUF2	-	-	-	-	-	-	-	PBHT
R/W	-	-	-	-	-	-	-	R/W
RESET	-	-	-	-	-	-	-	1

PBHT : *PortA7~4 buffer setting*

PBHT = 0 : CMOS input pin.

PBHT = 1 : Schmit input pin.

◆ **IOSK1**(0X174) : ***I/O Buffer Setting Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IOSK1	PA23S	PA01S	PB7S	PB6S	PB45S	PB23S	PB1S	PB0S
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

PA23S : *PortA.2/ PortA.3 Output Sink Enhancer enable*

PA01S : *PortA.0/ PortA.1 Output Sink Enhancer enable*

PB7S : *PortB.7 Output Sink Enhancer enable*

PB6S : *PortB.6 Output Sink Enhancer enable*

PB45S : *PortB.4/ PortB.5 Output Sink Enhancer enable*

PB23S : *PortB.2/ PortB.3 Output Sink Enhancer enable*

PB1S : *PortB.1 Output Sink Enhancer enable*

PB0S : *PortB.0 Output Sink Enhancer enable*

PxxS = 0 : Disable output sink Enhancer.

PxxS = 1 : Enable output sink Enhancer.

◆ **IOBUF1**(0X175) : ***I/O Buffer Setting Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IOBUF1	PA23T	PA01T	PB7T	PB6T	PB45T	PB23T	PB1T	PB0T
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

PA23T : *PortA.2/ PortA.3 input buffer setting*
PA01T : *PortA.0/ PortA.1 input buffer setting*
PB7T : *PortB.7 input buffer setting*
PB6T : *PortB.6 input buffer setting*
PB45T : *PortB.4/ PortB.5 input buffer setting*
PB23T : *PortB.2/ PortB.3 input buffer setting*
PB1T : *PortB.1 input buffer setting*
PB0T : *PortB.0 input buffer setting*

PxxT = 0 : CMOS input pin.
PxxT = 1 : Schmit input pin.

◆ **IOTPS** (0x17A) : ***Analog/Digital Channel Selection***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IOTPS	ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

ADCSx : Analog or digital channel selection

ADCSx=0 , Digital Channel.
ADCSx=1 , Analog Channel.

◆ **LDOC** (0x17B) : ***LDO Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LDOC	LDOS	LDWE	LDSE	LDOP	-	0	-	-
R/W	R/W	R/W	R/W	R/W	-	R/W	-	-
RESET	0	0	0	0	-	0	-	-

LDOS : LDO Setting Selection

LDOS=0 , By Option Code.

LDOS=1 , Set by LDOC Bit6~0.

LDWE : LDO Enable/disable while MCU operating.

LDWE=0 , Enable.

LDWE=1 , Disable.

LDSE : LDO Enable/disable while MCU sleeping.

LDSE=0 , Enable.

LDSE=1 , Disable.

LDOP : LDO/OP Selection.

LDOP=0 , LDO.

LDOP=1 , OP.

Bit2 : Please set to 0 fixed value.

◆ **LVRC** (0x17D) : ***Low Voltage Reset Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LVRC	LVRE	LVRD	LVRDI	LVFC1	LVFC0	LVS2	LVS1	LVS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	1	1	1

LVRE : ***Low Voltage Reset Enable***

TVRE=0 , LVR Enable .

TVRE=1 , LVR Disable.

LVRD : Low Voltage Pulse Detection.

LVRD=0 , Not Detected .

LVRD=1 , Detected .

LVRDI : Low Voltage Detection Interrupt Enable.

LVRDI=0 , Disable .

LVRDI=1 , Enable .

LVFC1~C0 : ***Low Voltage Reset Filter Clock Source***

LVCF1	LVCF0	Clock Source
0	0	No Filter
0	1	Trigger Pulse > 220us
1	0	Trigger Pulse > 480us
1	1	Trigger Pulse > 960us

LVS2~0 : ***Low Voltage Reset DetectionLevel***

000 , 2.0V .

Others , It's depends on LDO Level .

◆ **INTF** (0x17F) : ***Interrupt Flag Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTF	WDTIF	-	-	ICIF	TR1IF	SPIIF	EXIF	TR0IF
R/W	R/W	-	-	R/W	R/W	R/W	R/W	R/W
RESET	0	-	-	0	0	0	0	0

WDTIF : Watchdog timer overflow flag.

WDTIF = 0 , Clear it by Software.

WDTIF = 1 , If Watchdog timer overflow , this flag will be set to '1'.

ICIF : Port Change Interrupt flag.

ICIF = 0 , Clear it by Software.

ICIF = 1 , If port change interrupted , this flag will be set to '1'.

TR1IF : Timer 1 overflow flag.

TR1IF = 0 , Clear it by Software.

TR1IF = 1 , When Timer 1 overflow , this flag will be set to '1'.

SPIIF : SPI interrupt flag.

SPIIF = 0 , Clear it by Software.

SPIIF = 1 , Will be set when SPI interface interrupt occurred.

EXTIF : External interrupt flag.

EXTIF = 0 , Clear it by Software.

EXTIF = 1 , Will be set when the external interrupt occurred.

TR0IF : Timer 0 overflow flag.

TR0IF = 0 , Clear it by Software.

TR0IF = 1 , When Timer 0 overflow , this flag will be set to '1'.

3.0 Instruction Sets.

3.1 Overview

INSTRUCTION	DESCRIPTION	STATUS AFFECTED
NOP	No Operation	None
DAW	Decimal Adjust A	C
SLEEP	Go into Standby mode	T,P
WDTC	Clear Watchdog Timer	T,P
ENI	Enable Interrupt	None
DISI	Disable Interrupt	None
CLRW	Clear A	Z
CLR R	Clear R	Z
RETURN	Return from Subroutine	None
RETINT	Return from Interrupt	None
RETLW k	Return with literal in A	None
CALL k	Call Subroutine	None
JMP k	Jump to Address	None
MOV R,W	Move A to R	None
MOV W,R	Move R to A	Z
MOV R,R	Move R to R	Z
MOV W,k	Move literal to A	None
MOVC W,k	Move PAL, PAH ROM Data --> A	None
SWAPW R	Swap nibbles in R, ----> A	None
SWAP R	Swap nibbles in R, ----> R	None
BCR R,b	Bit Clear R	None
BSR R,b	Bit Set R	None
BTSC R,b	Bit Test R, Skip if Clear	None
BTSS R,b	Bit Test R, Skip if Set	None
RRCW R	Rotate Right R Through Carry ,----> A	C
RRC R	Rotate Right R Through Carry ,----> R	C
RLCW R	Rotate Left R Through Carry ,----> A	C

3.1 Overview (Continue)

INSTRUCTION	DESCRIPTION	STATUS AFFECTED
RLC R	Rotate Left R Through Carry ,----> R	C
AND W,R	A AND R ---> A	Z
AND R,W	A AND R ---> R	Z
AND W,k	A AND k ---> A	Z
OR W,R	A OR R ---> A	Z
OR R,W	A OR R ---> R	Z
OR W,k	A OR k ---> A	Z
XOR W,R	A XOR R ---> A	Z
XOR R,W	A XOR R ---> R	Z
XOR W,k	A XOR k ---> A	Z
INVW R	/R ---> A	Z
INV R	/R ---> R	Z
ADD W,R	A + R ---> A	Z,C,DC
ADD R,W	A + R ---> R	Z,C,DC
ADD W k	k+A ---> A	Z,C,DC
SUB W,R	R-A ---> A	Z,C,DC
SUB R,W	R-A ---> R	Z,C,DC
SUB W,k	k-A ---> A	Z,C,DC
INCW R	R+1 ---> A	Z
INC R	R+1 ---> R	Z
DECW R	R-1 ---> A	Z
DEC R	R-1 ---> R	Z
IRSZW R	R+1 ----> A, Skip if A=0	None
IRSZR R	R+1 ----> A, Skip if R=0	None
DRSZW R	R-1 ---> A, Skip if A=0	None
DRSZR R	R-1 ---> R, Skip if R=0	None

3.2 General Control Instructions

NOP	*No Operation*
Operation	NOP
Instruction Cycle	2
Affected Flag	None
Description	No any operation
Example	NOP

DAW	*Decimal Adjust*
Operation	If W[3:0]>9 or DC=1 Then W[3:0]+6 --> W[3:0] If W[7:4]>9 or C=1 Then W[7:4]+6 --> W[7:4]
Instruction Cycle	2
Affected Flag	C
Description	W Register Decimal Adjust & Place Result in W Register
Example	MOV W,@0x0E ; W=0x0EH DAW ; W=0x14H

SLEEP	*Sleep*
Operation	0--> WDT; Oscillator Stop
Instruction Cycle	2
Affected Flag	T,Z
Description	Clear Watch Dog Timer; then MCU Sleep
Example	SLEEP

WDTC	*Watch Dog Timer Clear*
Operation	0--> WDT;
Instruction Cycle	2
Affected Flag	T,P
Description	Clear Watch Dog Timer
Example	WDTC

ENI	*Enable Interrupt*
Operation	MCR/GIE Flag=0
Instruction Cycle	2
Affected Flag	None
Description	Enable Interrupt
Example	DISI

DISI	*Disable Interrupt*
Operation	MCR/GIE Flag=1
Instruction Cycle	2
Affected Flag	None
Description	Disable Interrupt
Example	DISI

CLR W	*Clear Working Register*
Operation	0 --> W
Instruction Cycle	2
Affected Flag	Z=1
Description	Clear Working Register Content --> W=0
Example	; before W=5AH CLR W ; after W=0H

CLR R	*Clear Register*
Operation	0 --> R
Instruction Cycle	2
Affected Flag	Z=1
Description	Clear Register Content --> R=0
Example	; before 0x10=5AH CLR 0x10 ; after 0x10=0H

3.3 Flow Control Instructions

RETURN	***Return from Subroutine.***
Operation	(Top Stack)--> PC,
Instruction Cycle	4
Affected Flag	None
Description	Return from Subroutine ; POP The Address from Top Stack
Example	SUB2: ; Subroutine 2. NOP NOP **RET** ; Return to LAB4 Addr. ; LAB3: NOP NOP CALL SUB2 ; go to SUB2 LAB4: NOP

RETINT	***Return from Interrupt.***
Operation	(Top Stack)--> PC, MCR/GIE Flag=1
Instruction Cycle	4
Affected Flag	None
Description	Return from Interrupt ; POP The Address from Top Stack
Example	ORG 0001H JMP SF_INT NOP SF_INT: NOP **RETINT** ; Feedback to LAB1 Main: NOP INT ; Software Interrupt ; go to 0001H Addr. LAB1 NOP ; ; Push LAB1 to Top Stack

RETLW	*Return with literal in W(Accumulator).*
Operation	(Top Stack)--> PC, MCR/GIE Flag=1
Instruction Cycle	4
Affected Flag	None
Description	Return from Interrupt ; POP The Address from Top Stack
Example	ORG 0001H JMP SF_INT NOP SF_INT: NOP **RETINT** ; Feedback to LAB1 Main: NOP INT ; Software Interrupt ; go to 0001H Addr. LAB1 NOP ; ; Push LAB1 to Top Stack

CALL k	*Call Subroutine*
Operation	K --> PC, (PC+1) --> (Top Stack)
Instruction Cycle	4
Affected Flag	None
Description	Call Subroutine, go to k Address(PC); Push the PC+1 to Top Stack
Example	**CALL** SUB1 ; go to SUB1 Addr. NOP NOP SUB1: ;

JMP k	*Jump to Assigned Addr.*
Operation	K --> PC,
Instruction Cycle	4
Affected Flag	None
Description	Go to k Address(PC);
Example	**JMP** LAB2 ; go to LAB2 Addr. NOP NOP LAB2: ;

3.4 Data Move Instructions

MOV R, W	*Write W Register to R Register*
Operation	W --> R
Instruction Cycle	2
Affected Flag	None
Description	Copy W Register Data to R Register
Example	NOP ; before W = 10, 0x20=0 MOV 0x20, W ; after W=10 , 0x20=10

MOV W, R	*Write R Register to W Register*
Operation	R --> W
Instruction Cycle	2
Affected Flag	Z
Description	Copy R Register Data to W Register
Example	NOP ; before W = 10, 0x25=15 MOV W, 0x25 ; after W=15 , 0x25=15

MOV R, R	*Writer R Register to itself*
Operation	R --> R
Instruction Cycle	2
Affected Flag	Z
Description	Copy R Register Data to R Register For check R Register is Zero or Not If Zero then Z flag=1

Example	; before 0x20=10
	..... ; 0x21=0
	MOV 0x20, 0x20 ; 0x20=10, Z=0
	MOV 0x21, 0x21 ; 0x21=0, Z=1

MOV W, k	*Writer a constant to W Register*
Operation	k --> W
Instruction Cycle	2
Affected Flag	None
Description	Copy W Register Data to R Register

Example	; before W = 10
	MOV W, @0x12 ; after W=12H
	MOV W, @01001010 ; W=4AH

MOVC	*Write ROM Data to W Register*
Operation	ROM Addr. [6:0]=PAL[7:1] ROM Addr. [11:7]=PAH[5:0] if PAL[0]='0'b then ROM[7:0]-->W if PAL[0]='1'b then ROM[15:8]-->W
Instruction Cycle	2
Affected Flag	None
Description	Read the ROM Data to W Register

Example	NOP ; Read Addr 100H ROM Data
	; ROM Addr.100H=0x1234
	
	MOV W,@0x00 ;
	MOV PAL,W
	MOV W,@0x02
	MOV PAH,W
	MOVC ;W=0x34 Read Low Byte
	MOV W@0x01
	MOV PAL,W
	MOVC ;W=0x12 Read High Byte

SWAPW R	*Swap R; Place Result in W Register*
Operation	R[3:0] --> W[7:4], R[7:4] --> W[3:0]
Instruction Cycle	2
Affected Flag	None
Description	Swap R Register High Nibble and Low Nibble & Place Result in W Register
Example	; before W = 10, 0x10=5A SWAPW 0x10 ; after W=A5, 0x10=5A

SWAP R	*Swap R*
Operation	R[3:0] <--> R[7:4]
Instruction Cycle	2
Affected Flag	None
Description	Swap R Register High Nibble and Low Nibble & Place Result in R Register
Example	; before 0x10=5A SWAPW 0x10 ; after 0x10=A5

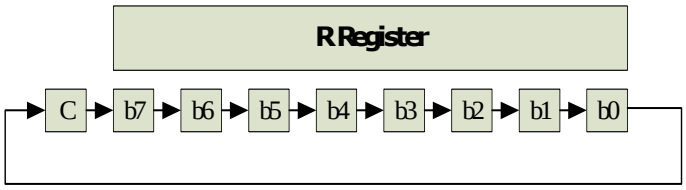
3.5 Bit Operate Instructions

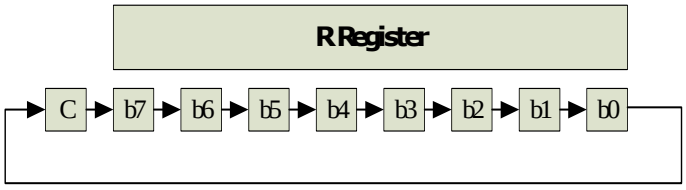
BCR R, b	*Clear Bit of Register*
Operation	0 --> R[b]
Instruction Cycle	2
Affected Flag	None
Description	Clear Assigned Bit of Register R[b]='0'b
Example	; before 0x10=5AH BCR 0x10,3 ; after 0x10=52H

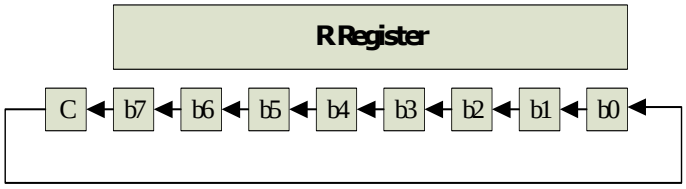
BSR R, b	*Set Bit of Register*
Operation	1 --> R[b]
Instruction Cycle	2
Affected Flag	None
Description	Set Assigned Bit of Register R[b]='1'b
Example	; before 0x10=5AH BSR 0x10,2 ; after 0x10=5EH

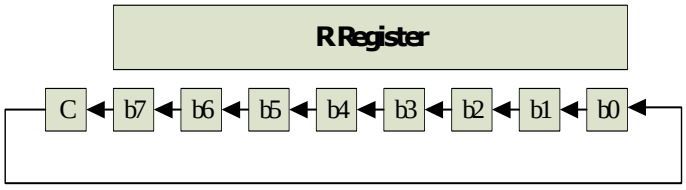
BTSC R, b	*Bit Test, Skip if Clear*
Operation	if R[b]=0 then Skip
Instruction Cycle	4
Affected Flag	None
Description	Bit Test; If this Bit is Clear, then Skip next instruction.
Example	; 0x20=01011010b ; 0x20 Bit2 ='0'b **BTSC** 0x20,2 ;Skip to NEXT2 NEXT1: JMP LAB1 NEXT2: JMP LAB2 LAB1: MOV W,@0AH LAB2: MOV W,@0BH ;

BTSS R, b	*Bit Test, Skip if Set*
Operation	if R[b]=1 then Skip
Instruction Cycle	4
Affected Flag	None
Description	Bit Test; If this Bit is Set, then Skip next instruction.
Example	; 0x20=01011010b ; 0x20 Bit3 ='1'b **BTSS** 0x20,1 ;Skip to NEXT2 NEXT1: JMP LAB1 NEXT2: JMP LAB2 LAB1: MOV W,@0AH LAB2: MOV W,@0BH ;

RRCW R	*Rotate Right R through Carry*
Operation	R[n]->W[n-1], R[0]->C, C--> W[7]
Instruction Cycle	2
Affected Flag	C
Description	 Place The Result in W Register
Example	; before W=0H , 0x10=5AH,C=1 RLCW 0x10 ; after W=ADH , 0x10=5AH,C=0

RRC R	*Rotate Right R through Carry*
Operation	R[n]->R[n-1], R[0]->C, C--> R[7]
Instruction Cycle	2
Affected Flag	C
Description	 Place The Result in R Register
Example	; before W=0H , 0x10=5AH,C=1 RLCW 0x10 ; after W=0H , 0x10=ADH,C=0

RLCW R	***Rotate Left R through Carry***
Operation	R[n]->W[n+1], R[7]->C, C--> W[0]
Instruction Cycle	2
Affected Flag	C
Description	 Place The Result in W Register
Example	; before W=0H , 0x10=5AH,C=1 RLCW 0x10 ; after W=B5H , 0x10=5AH,C=0

RLC R	***Rotate Left R through Carry***
Operation	R[n]->R[n+1], R[7]->C, C--> R[0]
Instruction Cycle	2
Affected Flag	C
Description	 Place The Result in R Register
Example	; before W=0H , 0x10=5AH,C=1 RLC 0x10 ; after W=0H , 0x10=B5H,C=0

3.6 Boolean Operate Instructions

AND W, R	*And logical operation*
Operation	W & R --> W
Instruction Cycle	2
Affected Flag	Z
Description	W Register & R Register & Place Result in W Register
Example	; before 0x10=5AH, W=0FH AND W,0x10 ; after 0x10=5AH, W=0AH

AND R, W	*And logical operation*
Operation	W and R --> R
Instruction Cycle	2
Affected Flag	Z
Description	W Register and R Register & Place Result in R Register
Example	; before 0x10=5AH, W=0FH AND 0x10, W ; after 0x10=0AH, W=0FH

AND W, k	*And logical operation*
Operation	W and k --> W
Instruction Cycle	2
Affected Flag	Z
Description	W Register and Constant k & Place Result in W Register
Example	; before W=A5H AND W, @0x0F ; after W=05H

OR W, R	*Inclusive OR logical operation*
Operation	W or R --> W
Instruction Cycle	2
Affected Flag	Z
Description	W Register or R Register & Place Result in W Register
Example	; before 0x10=5AH, W=0FH OR W,0x10 ; after 0x10=5AH, W=5FH

OR R, W	*Inclusive OR logical operation*
Operation	W or R --> R
Instruction Cycle	2
Affected Flag	Z
Description	W Register or R Register & Place Result in R Register
Example	; before 0x10=5AH, W=0FH OR 0x10, W ; after 0x10=5FH, W=0FH

OR W, k	*Inclusive OR logical operation*
Operation	W or k --> W
Instruction Cycle	2
Affected Flag	Z
Description	W Register or Constant k & Place Result in W Register
Example	; before W=A5H AND W, @0x0F ; after W=AFH

XOR W, R	*Exclusive OR logical operation*
Operation	W xor R --> W
Instruction Cycle	2
Affected Flag	Z
Description	W Register or R Register & Place Result in W Register
Example	; before 0x10=5AH, W=0FH XOR W,0x10 ; after 0x10=5AH, W=55H

XOR R, W	*Exclusive OR logical operation*
Operation	W xor R --> R
Instruction Cycle	2
Affected Flag	Z
Description	W Register xor R Register & Place Result in R Register
Example	; before 0x10=5AH, W=0FH XOR W,0x10 ; after 0x10=55H, W=0FH

XOR W, k	*Exclusive OR logical operation*
Operation	W xor k --> W
Instruction Cycle	2
Affected Flag	Z
Description	W Register xor Constant k & Place Result in W Register
Example	; before W=A5H AND W, @0x0F ; after W=AAH

3.7 Arithmetic Operate Instructions

INVW R	*Inverse Working Register*
Operation	/R --> W
Instruction Cycle	2
Affected Flag	Z
Description	Inverse Working Register Content W=/R
Example	; before W=0H ,0x10=5AH INVW 0x10 ; after W=A5H,0x10=5AH

INV R	*Inverse R Register*
Operation	/R --> R
Instruction Cycle	2
Affected Flag	Z
Description	Inverse Working Register Content W=/R
Example	; before W=0H , 0x10=5AH INV 0x10 ; after W=0H , 0x10=A5H

ADD W, R	*Add*
Operation	W+R --> W
Instruction Cycle	2
Affected Flag	Z,C,DC Z=1 ; when the Result =0 C=1 ; when the bit7 is Overflow DC=1; When the bit3 is Overflow
Description	W Register add R Register & Place Result in W Register

Example	; For R10 + R11--> W
	MOV W, 0x10 ; W=R10
	ADD W, 0x11 ; W=R10 +R11

ADD R, W	*Add*
Operation	W+R --> R
Instruction Cycle	2
Affected Flag	Z,C,DC Z=1 ; when the Result =0 C=1 ; when the bit7 is Overflow DC=1; When the bit3 is Overflow
Description	W Register add R Register & Place Result in R Register

Example	; For R10 + R11--> R11
	MOV W, 0x10 ; W=R10
	ADD 0x11, W ; R11=R10 +R11

ADD W, k	*Add*
Operation	W+k --> W
Instruction Cycle	2
Affected Flag	Z,C,DC Z=1 ; when the Result =0 C=1 ; when the bit7 is Overflow DC=1; When the bit3 is Overflow
Description	W Register add a constant & Place Result in W Register

Example	; For R10 + 15H --> W
	MOV W, 0x10 ; W=R10
	ADD W, @0x15 ; W=R10 +15H

SUB W, R	*Subtract*
Operation	R-W --> W
Instruction Cycle	2
Affected Flag	Z,C,DC Z=1 ; when the Result =0 ***C=0 ; when the bit7 is Overflow*** ***DC=0; When the bit3 is Overflow***
Description	R Register subtract W Register & Place Result in W Register

Example	; For R11- R10 --> W
	MOV W, 0x10 ; W=R10
	SUB W, 0x11 ; W=R11 – R10

SUB R, W	*Subtract*
Operation	R-W --> R
Instruction Cycle	2
Affected Flag	Z,C,DC Z=1 ; when the Result =0 ***C=0 ; when the bit7 is Overflow*** ***DC=0; When the bit3 is Overflow***
Description	R Register subtract W Register & Place Result in R Register

Example	; For R11- R10--> R11
	MOV W, 0x10 ; W=R10
	SUB 0x11, W ; R11=R11 -R10

SUB W, k	*Subtract*
Operation	k-W --> W
Instruction Cycle	2
Affected Flag	Z,C,DC Z=1 ; when the Result =0 ***C=0 ; when the bit7 is Overflow*** ***DC=0; When the bit3 is Overflow***
Description	A Constant subtract W Register & Place Result in W Register

Example	; For 15H – R10 --> W
	MOV W, 0x10 ; W=R10
	ADD W, @0x15 ; W=15H – R10

INCW R	*Increment R*
Operation	R+1 --> W
Instruction Cycle	2
Affected Flag	Z
Description	R Register Content add 1 & Place Result in W Register
Example	; before 0x10=5AH, W=0 INCW 0x10 ; after 0x10=5AH, W=5BH

INC R	*Increment R*
Operation	R+1 --> R
Instruction Cycle	2
Affected Flag	Z
Description	R Register Content add 1 & Place Result in R Register
Example	; before 0x10=5AH INC 0x10 ; after 0x10=5BH

DECW R	*Decrement R*
Operation	R-1 --> W
Instruction Cycle	2
Affected Flag	Z
Description	R Register Content subtract1 & Place Result in W Register
Example	; before 0x10=5AH, W=0 DECW 0x10 ; after 0x10=5AH, W=59H

DEC R	*Decrement R*
Operation	R-1 --> R
Instruction Cycle	2
Affected Flag	Z
Description	R Register Content subtract 1 & Place Result in R Register
Example	; before 0x10=5AH DEC 0x10 ; after 0x10=59H

IRSZW R	*Increment R, Skip if Zero.*
Operation	(R+1)-->W , Skip if result = 0
Instruction Cycle	4
Affected Flag	None
Description	Decrement R & Place the Result in W; If (R+1)=0 then Skip next instruction.
Example	; before 0x20=FFH **IRSZW** 0x20 ;W=0H,Skip NEXT2 NEXT1: JMP LAB1 NEXT2: JMP LAB2 LAB1: MOV W,@0AH LAB2: MOV W,@0BH ;

IRSZR R	*Increment R, Skip if Zero.*
Operation	(R+1)-->R , Skip if result = 0
Instruction Cycle	4
Affected Flag	None
Description	Increment R & Place the Result in R; If (R+1)=0 then Skip next instruction.
Example	; before 0x20=FFH **IRSZR** 0x20 ;0x20=0H,Skip NEXT2 NEXT1: JMP LAB1 NEXT2: JMP LAB2 LAB1: MOV W,@0AH LAB2: MOV W,@0BH ;

DRSZW R	*Decrement R, Skip if Zero.*
Operation	(R-1)-->W , Skip if result = 0
Instruction Cycle	4
Affected Flag	None
Description	Decrement R & Place the Result in W; If (R-1)=0 then Skip next instruction.
Example	; before 0x20=01H **DRSZW** 0x20 ;W=0H,Skip NEXT2 NEXT1: JMP LAB1 NEXT2: JMP LAB2 LAB1: MOV W,@0AH LAB2: MOV W,@0BH ;

DRSZR R	***Decrement R, Skip if Zero.***
Operation	(R-1)-->R , Skip if result = 0
Instruction Cycle	4
Affected Flag	None
Description	Decrement R & Place the Result in R; If (R-1)=0 then Skip next instruction.
Example	; before 0x20=01H **DRSZR** 0x20 ;0x20=0H,Skip NEXT2 NEXT1: JMP LAB1 NEXT2: JMP LAB2 LAB1: MOV W,@0AH LAB2: MOV W,@0BH ;

4.0 Device Configuration Options.

4.1 Protection

YSM343 have protection option to protect the code in MCU OTP ROM. If the protection option had been armed, there is no way to read back the data from OTP ROM.

4.2 Warm-up time

While the MCU is booting up, it will delay for specific time to wait for system stable. User can set up the time according to the slowest device in whole system to prevent timing issue error.

4.3 Power Save Mode(Eco-Mode)

YSM343 can reduce the power consumption by setting up this option. But limitation are existed for specific Eco-Mode level.

4.4 LDO (Low Drop Regulator)

YSM343 had an LDO module which can made the chip core operate in more wide range of the voltage. But the power consumption will little higher if the LDO module was being enabled.

4.5 System clock source selection

YSM343 had 6 types of the system clock source:

1. XTH – High speed external crystal (Frequency > 1MHz)
2. XTL – Low Speed external crystal (Frequency < 1MHz)
3. IRC w/o OSCO – Internal RC mode, no any outgoing clocks signal.
4. IRC w OSCO – Internal RC mode with the clock out on OSCO.
5. IRC w XTL – Internal RC mode with an external low speed crystal. The frequency of the low speed crystal is below 1MHz.
6. Ext. CLK OSCO – External clock source which input from OSCO.

Notes. OSCO output frequency can be set by option.
3 types of the OSCO frequency, Fosc/2, Fosc/4 and Fosc/8.

4.6 Low Voltage Reset

YSM343 had an Low Voltage Reset module, which can self reset the MCU if the operating voltage is lower than specific voltage level. User can specific the reference voltage and the continuous time period. If the voltage was below the reference voltage and keep for an period of the user specific, MCU will reset to avoid the low voltage issue error.

4.7 General MCU Functions

There are the following general MCU function can be setting in device configuration option.

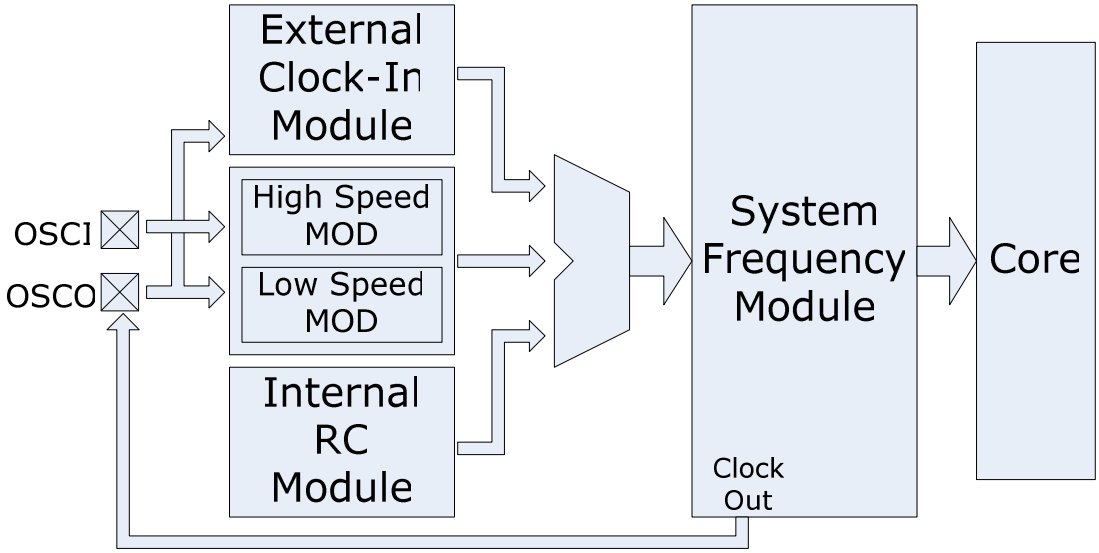
1. Watch Dog Timer : There is an internal RC clocked timer for watch dog function.

2. Auto Pull Setting : YSM343 have internal Pull up/down resistor for I/O ports. But if the output ports with internal pull up/down resistor connected, it will have the current leaking. If the Auto Pull Setting had been set, MCU will disconnect the pull up/down resistor while the ports being set to output to avoid the current leaking.

2. PB3/RSTN Setting : User can setting up the PB3 as normal pin or reset pin by setting up this option.

5.0 System Clock.

5.1 System clock overview



5.2 Clock source type

YSM343 have 3 different types of the clock source:

1. External crystal
2. Internal RC
3. External RC

5.3 External Crystal

User can use the standard 2 pins crystal(XTAL) with the internal clocking circuit to generate the precise frequency. The frequency can reach up to 16MHz.

5.4 Internal RC

YSM343 had build in an RC frequency generator on chip. User can select this module to generate an frequency clock signal for core use. It's no need to add any additional device to generate the clock signal. User can setting up to export the generated clock signal out from OSCO pin or not by device configuration.

5.5 External Clock Source

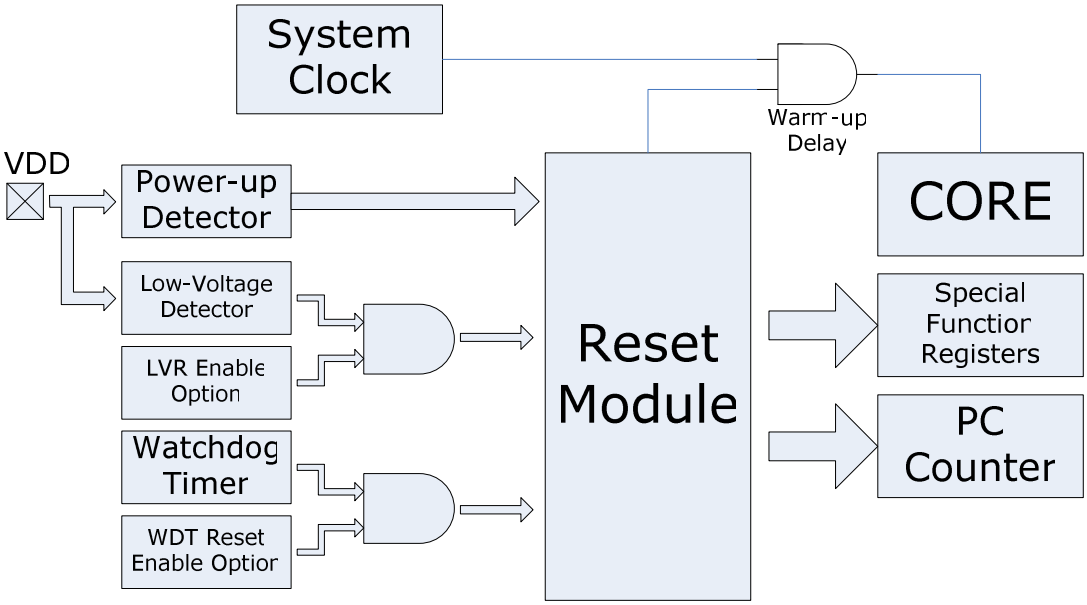
Except to the chip build-in RC frequency clock generator, user can connect to an external clock source from OSCO pin.

5.6 Clock signal export

YSM343 have an clock export module which can export an half frequency clock signal from the OSCO pin. This function was defined on the device configuration option.

6.0 Reset Module.

6.1 Overview



6.2 Power-On Reset

While the MCU had been power up, the MCU reset module will delay with the specific time period and reset the special function registers at the same time. The PC counter will also reset to address 0x000 while the power on reset. User can adjust the power up delay period (warm-up time) to wait the slower device in the designed system to avoid the timing issue error.

6.3 Low Voltage Reset (L.V.R)

M343 had build-in an low voltage detector. If the operating voltage (VDD)'s level is keep below the specific reference voltage level for an specific period, low voltage detector will send an reset signal to the reset module to reset the MCU. This function is used to avoid the operating error from the low voltage issue. If the LVR reset had been executed, the PC counter will be reset to 0x000.

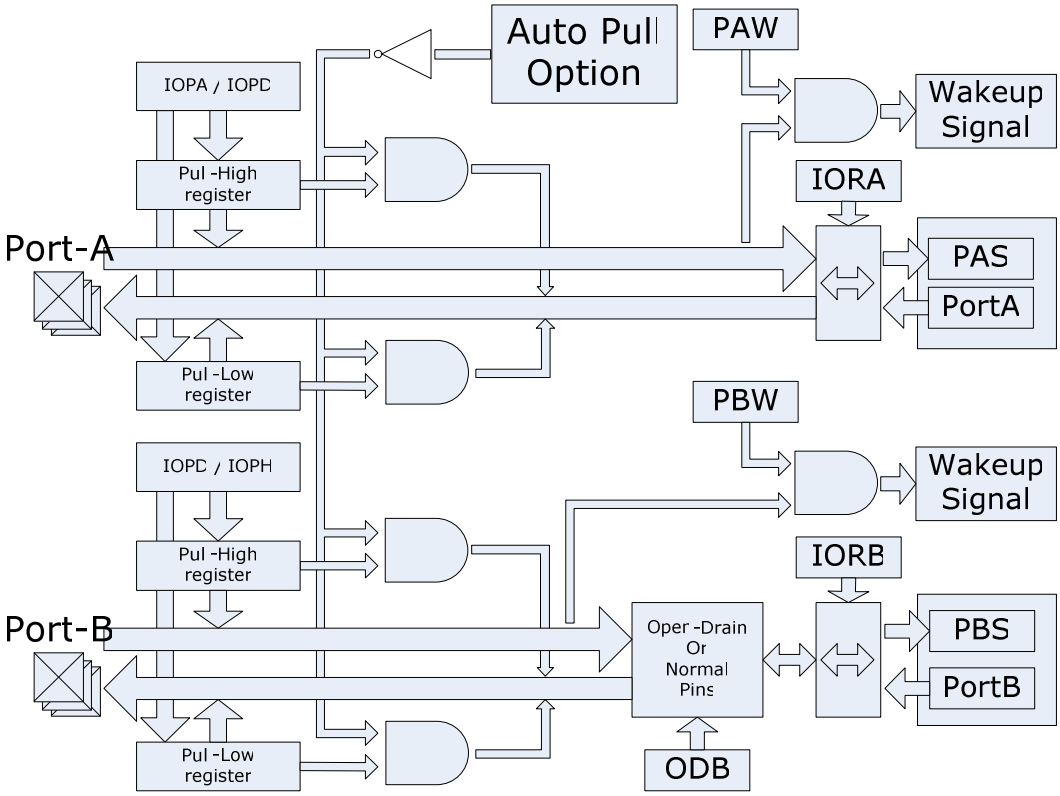
6.4 Watchdog Reset (WDT Reset)

YSM343 had a watchdog timer. If the watchdog timer had been enabled and the watchdog timer overflow flag was being set, it will send a reset signal to reset module to reset the MCU. The PC counter will be reset to 0x000. The watchdog timer reset is used to avoid the MCU hang on crash or infinite looping status.

Notes: User should clear up the watch dog timer regularly to avoid the WDT reset.

7.0 I/O Ports Module.

7.1 Overview



7.2 Ports

M343 have 2 I/O ports, which are Port-A and Port-B. Each port can be set to input or output. All ports are 8bits wide and can connect with the internal pull resistors.

There are 3 general power relative ports(VDD / VDDL / VSS)

1 External reset port is available, low active.

1 External interrupt pin with internal pull up.

2 frequency ports (OSCI / OSCO)

7.3 I/O Ports Direction Control

There are 2 ports in YSM343. Each one can be set to input or output by using the IORx special function register to control the port direction.

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IORA	IOA7	IOA6	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1
IORB	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

IOx0~7=0 , as a Output. / IOx0~7=1 , as a Input.

7.4 I/O Ports Value Write

User can output the port data via the PORTx special function registers and read the outputted data from these SFRs.

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PORTA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0
PORTB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

7.5 I/O Ports Value Read

User can read the pin status data via the PxS special function registers.

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PAS	PAS7	PAS6	PAS5	PAS4	PAS3	PAS2	PAS1	PAS0
R/W	R	R	R	R	R	R	R	R
RESET	-	-	-	-	-	-	-	-
PBS	PBS7	PBS6	PBS5	PBS4	PBS3	PBS2	PBS1	PBS0
R/W	R	R	R	R	R	R	R	R
RESET	-	-	-	-	-	-	-	-

PxS0~PxS7 : *I/O Port Reading Data From Pin Status.*

7.6 I/O Ports Pull resistors

◆ **IOPA** (0x12A) : ***Port A I/O Pull Resistor Setting***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IOPA	/PUA7	/PUA6	/PUA5	/PUA4	/PDA7	/PDA6	/PDA5	/PDA4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

/PUAx : *I/O pins Pull-high resistor*

/PUAx=0 , Enable the pull-high resistor(PortA7~4).

/PUAx=1 , Disable the pull-high resistor(PortA7~4).

/PDAx : *I/O pins Pull-low resistor*

/PDAx=0 , Enable the pull-down resistor(PortA7~4).

/PDAx=1 , Disable the pull-down resistor(PortA7~4).

◆ **IOPD** (0x12B) : ***I/O Port Pull Down Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IOPD	/PDB3	/PDB2	/PDB1	/PDB0	/PDA3	/PDA2	/PDA1	/PDA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

/PDA3~/PDA0 : ***Each I/O Port Pull-Down Enable Bit***

/PDAx=0 , Enable the pull-down resistor(PortA3~0).

/PDAx=1 , Disable the pull-down resistor(PortA3~0).

/PDB3~/PDB0 : ***Each I/O Port Pull-Down Enable Bit***

/PDBx=0 , Enable the pull-down resistor(PortB3~0).

/PDBx=1 , Disable the pull-down resistor(PortB3~0).

◆ **IOPH** (0x12D) : ***I/O Port Pull High Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IOPH	/PUB7	/PUB6	PUB5	/PUB4	/PUB3	/PUB2	/PUB1	/PUB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

/PUB7~/PUB0 : ***Each I/O Port Pull-Up Enable Bit***

/PUB7~/PUB0=0 , Enable (Connected with Pull High Resistor).

/PUB7~/PUB0=1 , Disable(disconnect with Pull High Resistor).

7.7 Port Change Wakeup Registers

◆ **PBW** (0x120) : ***Port B Wake Up Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PBW	WB7	WB6	WB5	WB4	WB3	WB2	WB1	WB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET								

WB7~0 : ***Port B PIN Wake Up Enable***

WB7~0=1 , Port B7~B0 can be the wakeup pins.

Wake Up Condition : As a Input Port & Input Signal from High to Low / Low to High.

WB7~0=0 , Disable.

(Continue)

I/O Port as a Wake Up PIN Setting Procedure:

Step 1: Setting as a Input PIN

Step 2: Pull Up/ Pull Down Enable .

Step 3: Enable Wake Up Function

Step 4: Enter to Sleep.

◆ **PAW** (0x121) : ***Port A Wake Up Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PAW	WA7	WA6	WA5	WA4	WA3	WA2	WA1	WA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET								

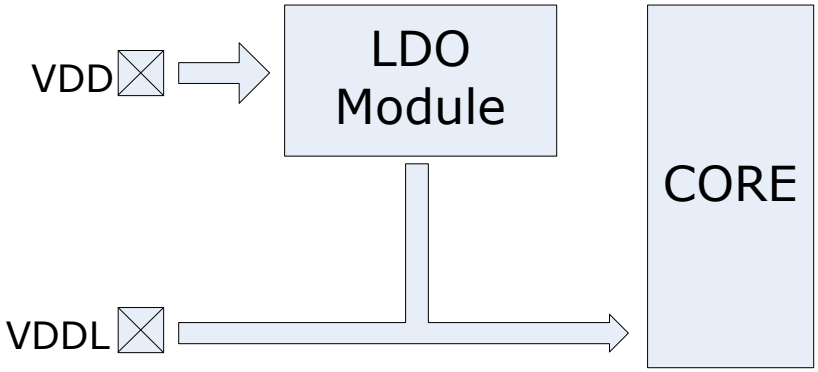
WA7~0 : *Port A PIN Wake Up Enable*

WA7~0=1 , Port A7~A0 can be wake –up

Wake Up Condition : As a Input Port & Input Signal from High to Low / Low to High.

WA7~0=0 , Disable.

7.6 Power Relative Pins



VDD and VDDL should connect to an 0.1uF capacitor each.

7.7 External Interrupt Pin

User can trig the external interrupt by set low to the external interrupt pin with internal pull up.

8.0 Chip Status.

8.1 Overview

The status flags are being build in the YSM343's special function registers. User can know the status of the MCU by monitor the register.

8.2 Status Register

◆ **STATUS** (0x103) : ***Status Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STATUS	GPR	-	-	/TO	/PD	Z	DC	C
R/W	R/W			R/W	R/W	R/W	R/W	R/W
RESET								

GPR : ***General Purpose Read/Write bit***

/TO : ***Time- Out Flag***

/TO=0 Watch dog Timer Overflow.

/TO=1 (a) Power On

(b) Execute WDTC or SLEEP Instruction.

/PD : ***Power Down Flag***

/PD=0 After SLEEP Instruction.

/PD=1 (a) Power On

(b) Execute WDTC Instruction.

Z : ***ALU Operation Zero Flag***

Z=0 Operation Result is not Zero.

Z=1 Operation Result is Zero.

DC : ***ALU Operation Half Carry /Borrow Flag***

DC=0 Half Carry/Borrow does not occur.

DC=1 Half Carry/Borrow occurred.

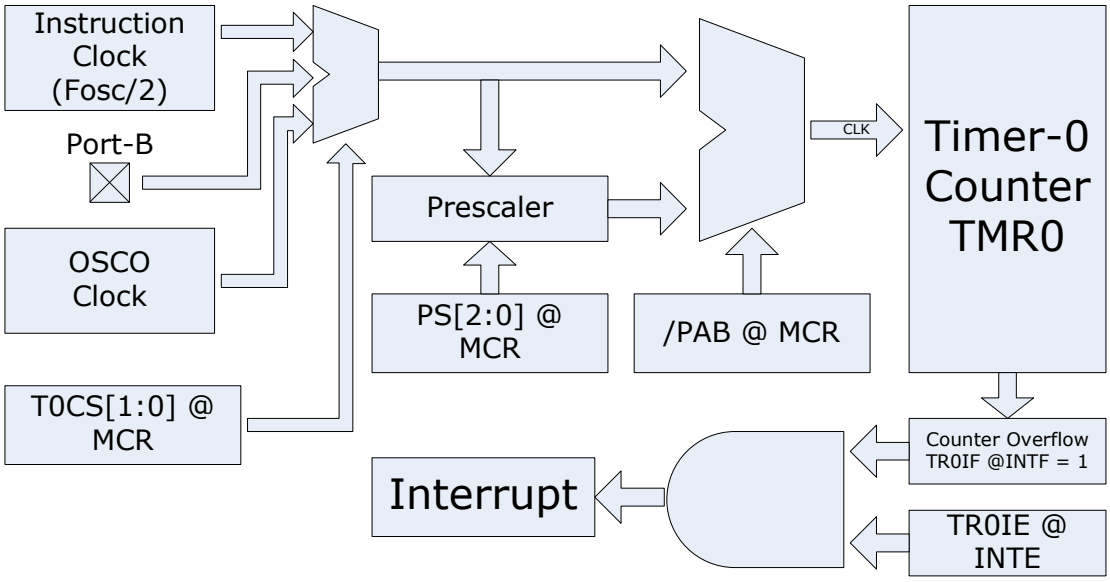
C : ***ALU Operation Carry /Borrow Flag***

C=0 Carry/Borrow does not occur.

C=1 Carry/Borrow occurred.

9.0 Timer0.

9.1 Overview



9.2 Registers

◆ **MCR** (0x122) : ***Main Control Register for Read / Write***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MCR	T0CS1	GIE	T0CS0	TM0CE	PAB	PS2	PS1	PS0
R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	0	1	1	1	1	1	1

T0CS1~T0CS0 : ***Timer-0 Clock Source .***

T0CS1	T0CS0	Timer 0 Clock Source
1	1	Instruction cycle(Fosc/2)
1	0	External TCC clock (PB2)
0	1	OSCO clock
0	0	Reserved

TM0CE : ***Timer-0 Counting edge while using external TCC.***

TM0CE=0 Timer-0 increasing at TCC rising edge.

TM0CE=1 Timer-0 increasing at TCC falling edge.

PAB : ***Prescaler bit Assignment .***

PAB=0 Assign to TMR0 (Timer 0).

PAB=1 Assign to WDT (Watch-Dog Timer).

PS2~PS0 : ***Prescaler bits.***

PS2	PS1	PS0	TMR0 Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

When The TMR0 from 0xff increasing to 0x00 , TR0IF will be set to '1', and if the TR0IE=1 , then the Program Counter will go to Address 0x009(Timer 0 Overflow Interrupt Address).

◆ **TMR0** (0x101) : ***8Bits Real Timer Clock/Counter***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TMR0	8 bit Real Time Clock / Counter							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

TMR0 : Increased By Instruction Cycle.

◆ **INTE** (0x12F) : ***Hardware Interrupt Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTE	WDTIE	-	-	ICIE	TR1IE	SPIIE	EXIE	TR0IE
R/W	R/W	-	-	R/W	R/W	R/W	R/W	R/W
RESET	0	-	-	0	0	0	0	0

TR0IE : *Timer 0 Interrupt Enable*

TR0IE=0 , Timer 0 Interrupt Disable .

TR0IE=1 , Timer 0 Interrupt Enable .

◆ **INTF** (0x17F) : ***Interrupt Flag Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTF	WDTIF	-	-	ICIF	TR1IF	SPIIF	EXIF	TR0IF
R/W	R/W	-	-	R/W	R/W	R/W	R/W	R/W
RESET	0	-	-	0	0	0	0	0

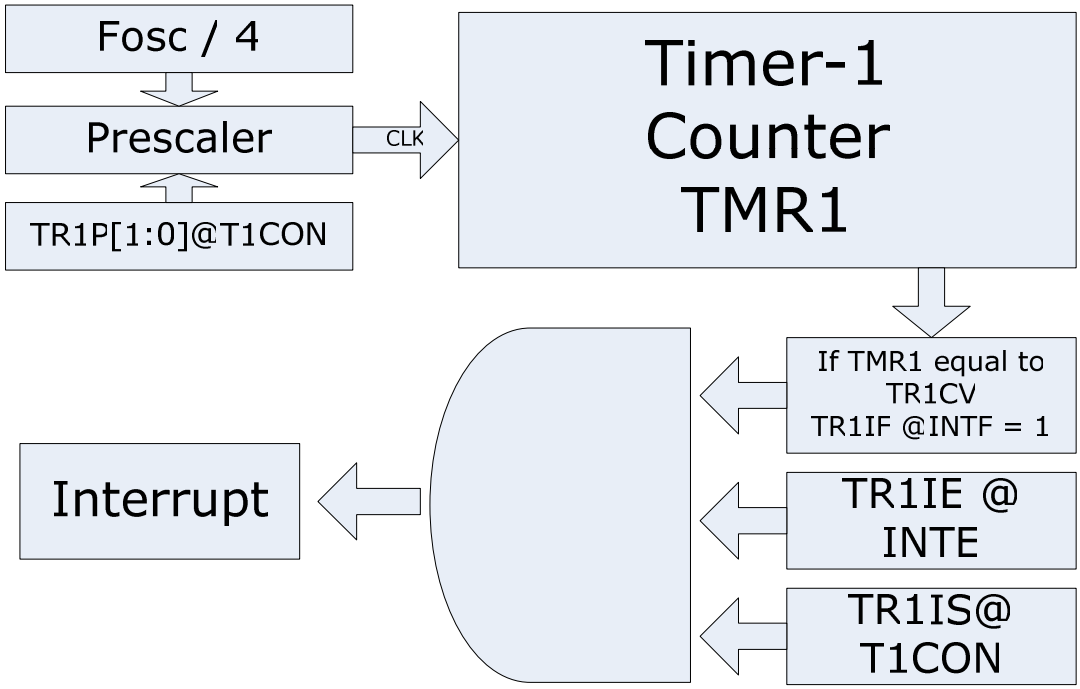
TR0IF : Timer 0 overflow flag.

TR0IF = 0 , Clear it by Software.

TR0IF = 1 , When Timer 0 overflow , this flag will be set to '1'.

10.0 Timer1.

10.1 Overview



10.2 Registers

Timer1 is an 8 bits timer. When set the TR1IE=1, TR1S=1 , the Timer1 will count from 0x00(TMR1).

If the Register TMR1 equal to the register TR1CV, the TR1IF will be set to 1 and the program counter will go to Address 0x011(Hardware Interrupt Address) .

◆ **INTE** (0x12F) : ***Hardware Interrupt Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTE	WDTIE	-	-	ICIE	TR1IE	SPIIE	EXIE	TR0IE
R/W	R/W	-	-	R/W	R/W	R/W	R/W	R/W
RESET	0	-	-	0	0	0	0	0

TR1IE : *Timer 0 Interrupt Enable*

TR1IE=0 , Timer 1 Interrupt Disable .

TR1IE=1 , Timer 1 Interrupt Enable .

◆ **INTF** (0x17F) : ***Interrupt Flag Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTF	WDTIF	-	-	ICIF	TR1IF	SPIIF	EXIF	TR0IF
R/W	R/W	-	-	R/W	R/W	R/W	R/W	R/W
RESET	0	-	-	0	0	0	0	0

TR1IF : Timer 0 overflow flag.

TR1IF = 0 , Clear it by Software.

TR1IF = 1 , When TMR1 = TR1CV, this flag will be set to '1'.

◆ **TMR1** (0x13E) : ***Timer 1 Value Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TMR1	Timer 1 Value Register							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

◆ **TR1CV** (0x13F) : ***Timer 1 Comparator Value Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TR1CV	Timer 1 Comparator Value Register							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

◆ **T1CON** (0x12C) : ***Timer 1 Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
T1CON	-	-	-	-	-	TR1S	TR1P1	TR1P0
R/W						R/W	R/W	R/W
RESET								

TR1S : *Timer 1 Turn On Bit*

TR1S=0 , Timer 1 turn off.

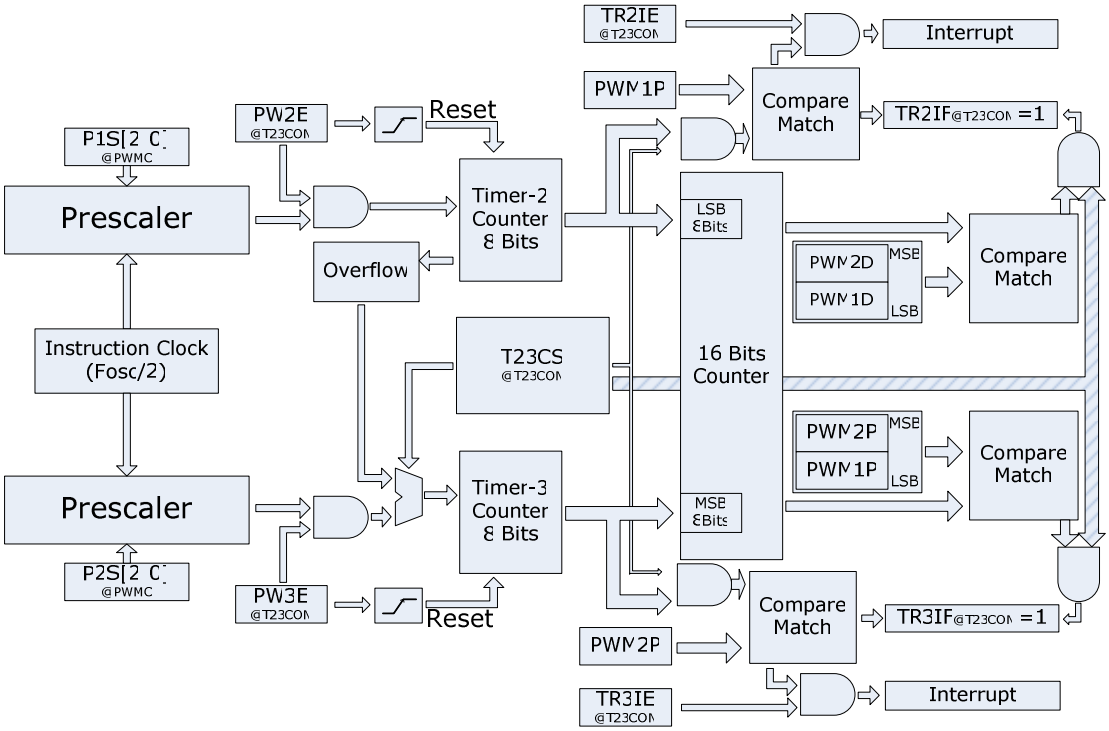
TR1S=1 , Timer 1 turn on.

TR1P1,TR1P0 : *Timer 1 Prescaler Rate*

TR1P1	TR1P0	TMR0 Rate
0	0	1:1
0	1	1:4
1	0	1:8
1	1	1:16

11.0 Timer2 / Timer3.

11.1 Overview



11.2 Registers

◆ **T23CON** (0x135) : ***Timer Setting and PWM Setting Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
T23CON	TR2S	TR2IE	TR2IF	TR3S	TR3IE	TR3IF	POINV	T23CS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

TR2S : *Timer 2 Enable*

TR2S=0 , Timer 2 Disable.

TR2S=1 , Timer 2 Enable.

TR2IE : *Timer 2 Interrupt Enable*

TR2IE=0 , Timer 2 Interrupt Disable.

TR2IE=1 , Timer 2 Enable.

TR2IF : *Timer 2 Interrupt Flag*

TR2IF=0 , Clear by software.

TR2IF=1 , Timer 2 interrupt occurred.

TR3S : *Timer 3 Enable*

TR3S=0 , Timer 3 Disable.

TR3S=1 , Timer 3 Enable.

TR3IE : *Timer 3 Interrupt Enable*

TR3IE=0 , Timer 3 Interrupt Disable.

TR3IE=1 , Timer 3 Enable.

TR3IF : *Timer 3 Interrupt Flag*

TR3IF=0 , Clear by software.

TR3IF=1 , Timer 3 interrupt occurred.

POINV : *PWM output invert*

POINV=0 , Initial with low level, high level PWM pulse.

POINV=1 , Initial with high level, low level PWM pulse.

T23CS : *Timer2 and Timer3 cascade mode*

T23CS=0 , Timer2 and Timer3 standalone mode.

T23CS=1 , Timer2 and Timer3 cascaded.

◆ **PWM1D** (0x130) : ***PWM1 Duty Cycle Data Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM1D	P1D7	P1D6	P1D5	P1D4	P1D3	P1D2	P1D1	P1D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

◆ **PWM2D** (0x131) : ***PWM2 Duty Cycle Data Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM2D	P2D7	P2D6	P2D5	P2D4	P2D3	P2D2	P2D1	P2D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

(Continue)

◆ **PWM1P** (0x132) : ***PWM1 Period Data Register***

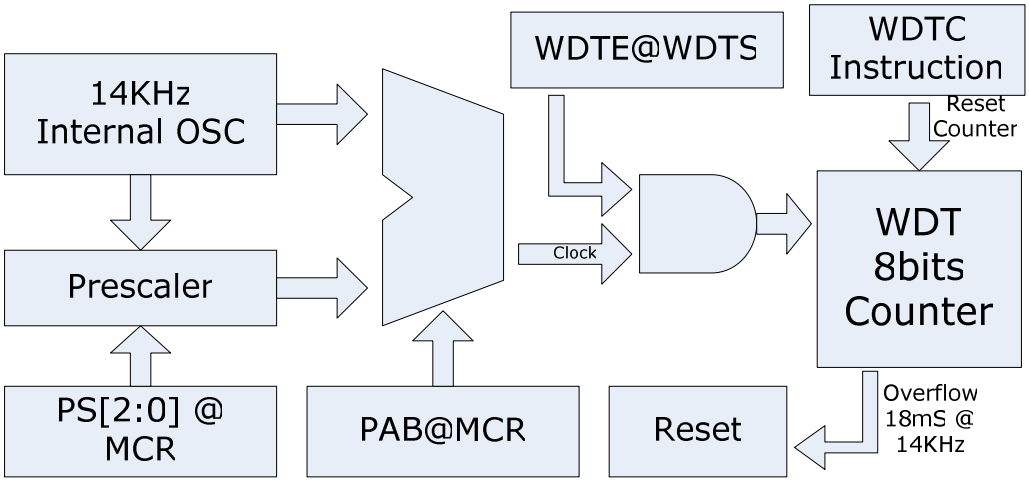
NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM1P	P1P7	P1P6	P1P5	P1P4	P1P3	P1P2	P1P1	P1P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

◆ **PWM2P** (0x133) : ***PWM2 Period Data Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM2P	P2P7	P2P6	P2P5	P2P4	P2P3	P2P2	P2P1	P2P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

12.0 Watchdog Timer.

12.1 Overview



12.2 Registers

◆ **MCR** (0x122) : ***Main Control Register for Read / Write***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MCR	T0CS1	GIE	T0CS0	TM0CE	PAB	PS2	PS1	PS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	0	1	1	1	1	1	1

PAB : ***Prescaler bit Assignment .***

PAB=0 Assign to TMR0 (Timer 0).

PAB=1 Assign to WDT (Watch-Dog Timer).

PS2~PS0 : ***Prescaler bits.***

PS2	PS1	PS0	TMR0 Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

◆ **WDTS** (0x12E) : ***Watch Dog & Wake Up Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WDTS	EIS	EIT	WDTE	SLP2E	WDCKS	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	-	-	-
RESET								

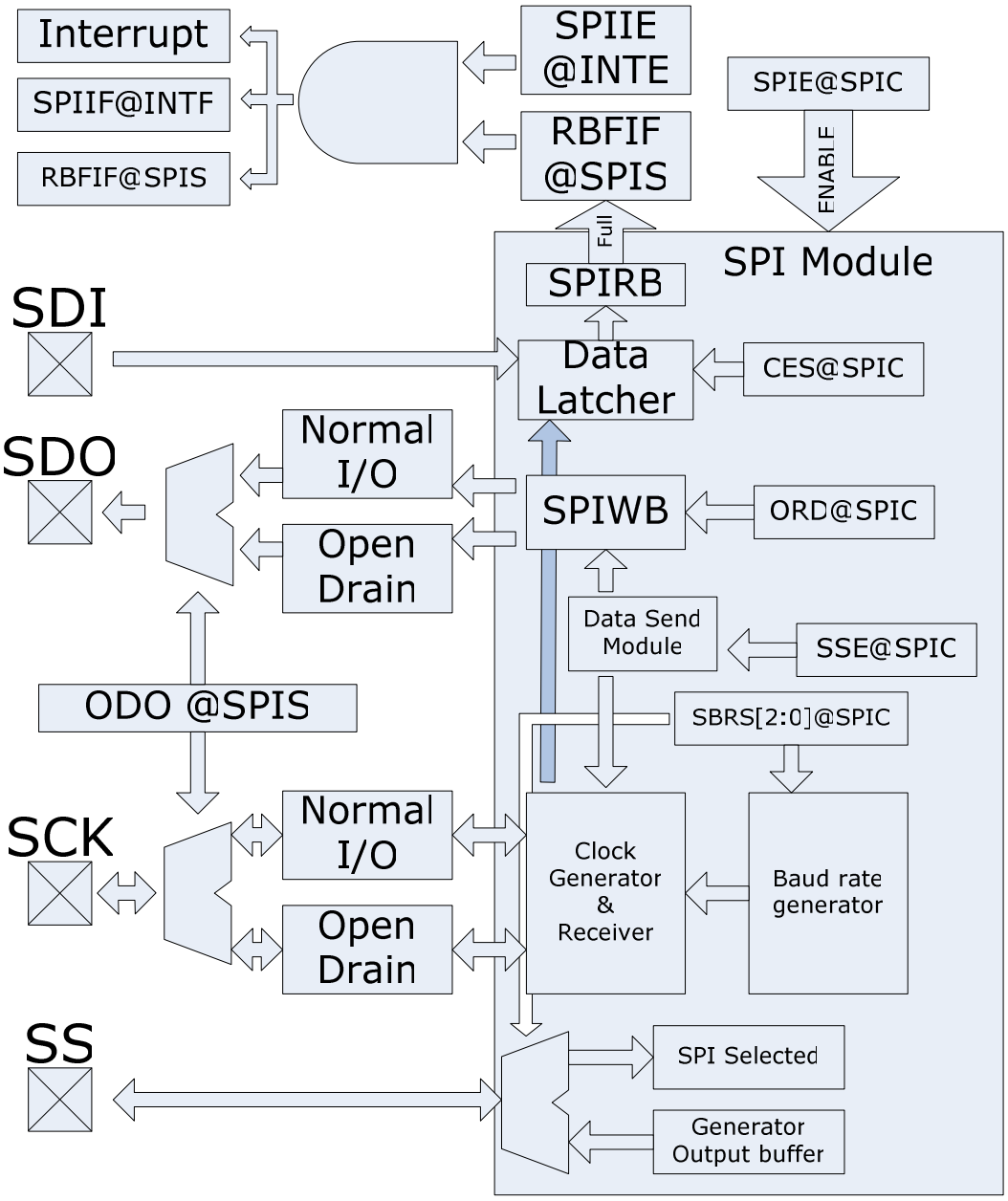
/WDTE : Watchdog timer Enable

/WDTE=0 , Watchdog timer disable .

/WDTE=1 , Watchdog timer enable.

13.0 SPI interface.

13.1 Overview



13.2 Registers

◆ **SPIC**(0X13D) : ***SPI Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIC	CES	SPIE	SRO	SSE	ORD	SBRS2	SBRS1	SBRS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	-	0	0	0	0

CES : *SPI Clock Edge Selection*

CES=0 , **Low go High** , Data Out; **High go Low** Data In.

CES=1 , **High go Low** , Data Out; **Low go High** Data In.

SPIE : *SPI Enable*

SPIE=0 ,SPI Disable.

SPIE=1 ,SPI Enable.

SRO : *Data In Overflow Flag (Only Used SLAVE Mode)*

SRO=1 ,Last Byte Data in SPI Read Buffer had not Read Out .

SRO=0 ,Otherwise.

SSE : *Start Shift SPI Data Out*

SSE=1 ,(a)Start Shift SPI Data Out.

(b) Completed Working , Clear SSE bit by Hardware .

SRO=0 ,Otherwise.

ORD : *SPI Data Shift Order*

ORD=0 ,MSB Bit First.

ORD=1 ,LSB Bit First.

SBRS2~SBRS0 : *SPI Baud Rate & Mode Selection*

SBRS2	SBRS1	SBRS0	Mode	Baud Rate
0	0	0	Master	Fosc/2
0	0	1	Master	Fosc/4
0	1	0	Master	Fosc/8
0	1	1	Master	Fosc/16
1	0	0	Master	Fosc/32
1	0	1	Slave	SS Enable
1	1	0	Slave	SS Disable
1	1	1	Master	TMR1/2

◆ **SPIS**(0X13C) : ***SPI Status Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIS	-	-	-	-	ODO	ODC	RBFIF	RBF
R/W-	-	-	-	-	R/W	R/W	R/W	R/W
RESET	-	-	-	-	0	0	0	0

ODO : ***SDO Open-Drain Control***

ODO=0 ,SDO Open-Drain Disable.

ODO=1 ,SDO Open-Drain Enable.

ODC : ***SCK Open-Drain Control***

ODC=0 ,SCK Open-Drain Disable.

ODC=1 ,SCK Open-Drain Enable.

RBFIF : ***SPI Read Buffer Full Interrupt Flag***

RBFIF=1 ,(a)Receive Completed, and Read Buffer is Full.
(b) Under the Interrupt Enable, and Interrupt Occur.

RBFIF=0 ,Receive Status is Ongoing , Read Buffer is Empty.

RBFIF : ***SPI Read Buffer Full Flag***

RBF=1 ,Receive Completed, and Read Buffer is Full.

RBF=0 ,Receive Status is Ongoing , Read Buffer is Empty.

◆ **SPIRB**(0X13A) : ***SPI Data Read Buffer***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIRB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

SPIRB Register is a 8 bits Data Buffer for SPI Data Read In.

◆ **SPIWB**(0X13B) : ***SPI Data Write Buffer***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIWB	WB7	WB6	WB5	WB4	WB3	WB2	WB1	WB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

SPIRB Register is a 8 bits Data Buffer for SPI Data Write Out.

◆ **INTE** (0x12F) : ***Hardware Interrupt Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTE	-	-	-	-	TR1IE	SPIIE	EXIE	TR0IE
R/W	-	-	-	-	R/W	R/W	R/W	R/W
RESET	-	-	-	-	0	0	0	0

SPIIE : *SPI Read Buffer Full Interrupt Enable*

SPIIE=0 , SPI Read Buffer Full Interrupt Disable .

SPIIE=1 , SPI Read Buffer Full Interrupt Enable .

◆ **INTF** (0x17F) : ***Interrupt Flag Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTF	-	-	-	-	TR1IF	SPIIF	EXIF	TR0IF
R/W	-	-	-	-	R/W	R/W	R/W	R/W
RESET	-	-	-	-	0	0	0	0

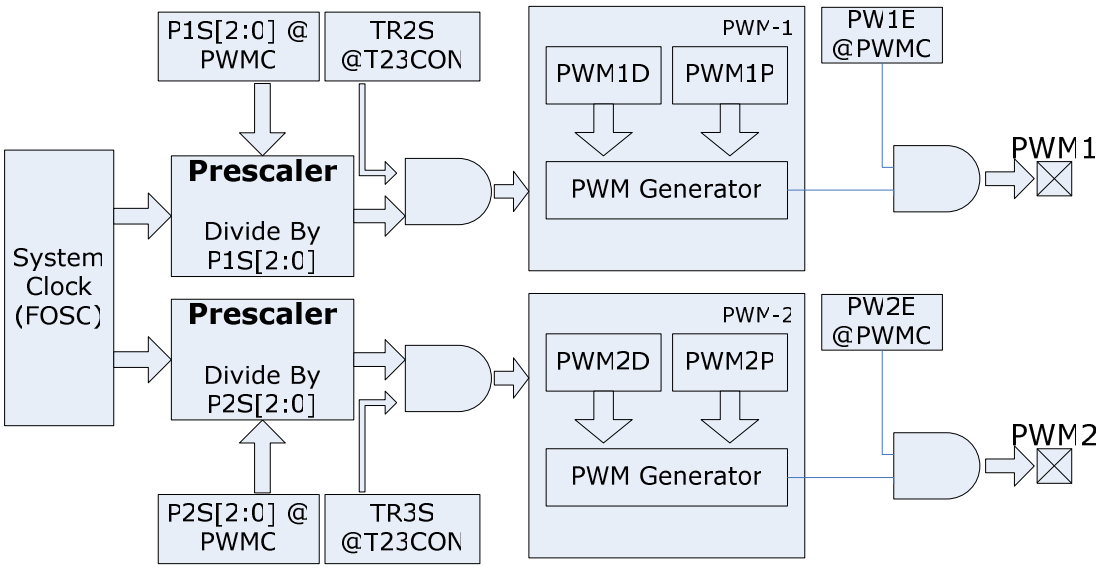
SPIIF : SPI Read Buffer Full Interrupt flag.

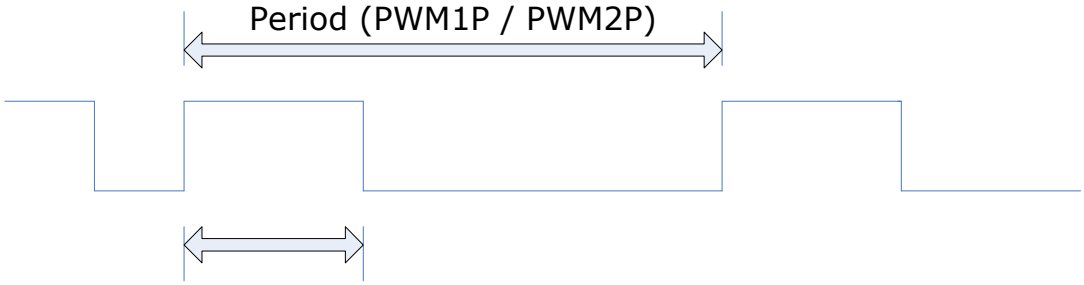
SPIIF = 0 , Clear it by Software.

SPIIF = 1 , When SPI read buffer full, this flag will be set to '1'.

14.0 PWM – Pulse Width Modulator.

14.1 Overview





Duty Cycle (PWM1D / PWM2D)

Duty Cycle = (PWMxD/PWMxP)*100%

14.2 Registers

◆ **PWMC** (0x134) : ***PWM Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWMC	PW2E	PW1E	P2S2	P2S1	P2S0	P1S2	P1S1	P1S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

PW2E : ***PWM2 Enable Bit***

PW2E=0 , PWM2 Disable.

PW2E=1 , PWM2 Enable.

PW1E : ***PWM1 Enable Bit***

PW1E=0 , PWM1 Disable.

PW1E=1 , PWM1 Enable.

PxS2,PxS1,PxS0 : ***PWM Clock Prescaler Rate(x = 1 or 2)***

PxS2	PxS1	PxS0	PWM Clock Rate
0	0	0	Fosc/2
0	0	1	Fosc/4
0	1	0	Fosc/8
0	1	1	Fosc/16
1	0	0	Fosc/32
1	0	1	Fosc/64
1	1	0	Fosc/128
1	1	1	Fosc/256

◆ **PWM1D** (0x130) : ***PWM1 Duty Cycle Data Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM1D	P1D7	P1D6	P1D5	P1D4	P1D3	P1D2	P1D1	P1D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

P1D7~P1D0 : ***8 bits PWM1 Duty Cycle Data***

◆ **PWM1P** (0x132) : ***PWM1 Period Data Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM1P	P1P7	P1P6	P1P5	P1P4	P1P3	P1P2	P1P1	P1P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

P1P7~P1P0 : ***8 bits PWM1 Period Data***

Note: PWM1 Signal Output fromPB6 PIN

◆ **PWM2D** (0x131) : ***PWM2 Duty Cycle Data Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM2D	P2D7	P2D6	P2D5	P2D4	P2D3	P2D2	P2D1	P2D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

P2D7~P2D0 : ***8 bits PWM2 Duty Cycle Data***

◆ **PWM2P** (0x132) : ***PWM2 Period Data Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM2P	P2P7	P2P6	P2P5	P2P4	P2P3	P2P2	P2P1	P2P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

P2P7~P2P0 : ***8 bits PWM2 Period Data***

Note: PWM2 Signal Output from PB7 PIN

◆ **T23CON** (0x135) : ***Timer Setting and PWM Setting Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
T23CON	TR2S	TR2IE	TR2IF	TR3S	TR3IE	TR3IF	POINV	T23CS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

TR2S : ***Timer 2 Enable***

TR2S=0 , Timer 2 Disable.

TR2S=1 , Timer 2 Enable.

(Continue)

TR3S : *Timer 3 Enable*

TR3S=0 , Timer 3 Disable.

TR3S=1 , Timer 3 Enable.

T23CS : *Timer2 and Timer3 cascade mode*

T23CS=0 , Timer2 and Timer3 standalone mode.

T23CS=1 , Timer2 and Timer3 cascaded.

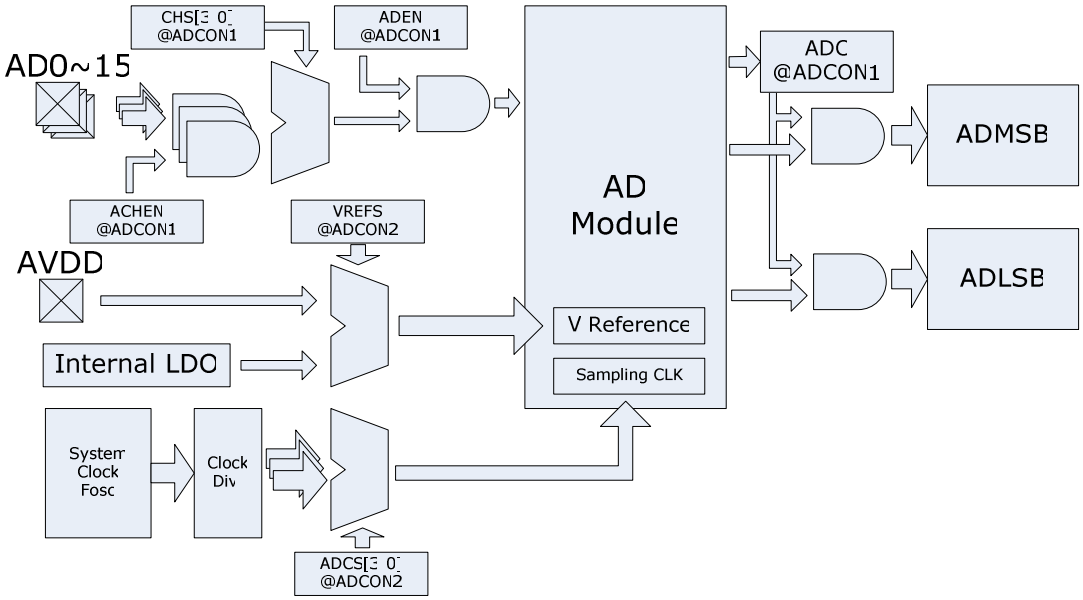
If user use 2 PWM modules, please set the timer2 and timer3 to standalone mode.

14.3 Code Setting Flow

```
MOV A,          @0X7F       ;Setup the PWM duty cycle register
MOV PWM1D,      A
MOV PWM2D,      A
MOV A,          @0XFF       ;Setup the PWM period data register
MOV PWM1P,      A
MOV PWM2P,      A
MOV A,          @0x02
MOV PWMC,       A           ; Set Prescaler to Fosc/8
BSR T23CON,     7           ; Enable PWM1 clock source
BSR T23CON,     6           ; Enable PWM2 clock source
BCR T23CON,     0           ; Set PWM clock to standalone mode
BSR PWMC,       6           ; Active the PWM-1 module
BSR PWMC,       7           ; Active the PWM-2 module
;Now the PWM-1 and PWM-2 start to output the PWM signal.
```

15.0 Analog to Digital Converter.

15.1 Overview



15.2 Registers

◆ **ADCON1**(0X140) : ***A/D Control Register #1***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADCON1	ADC	ADEN	ACHEN	-	CHS3	CHS2	CHS1	CHS0
R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
RESET	0	0	0	-	0	0	0	0

ADC : *ADC Start Transfer & Completed Flag*

ADC=0 , ADC is be Transfer Completed.(Clear by MCU Hardware)

ADC=1 , ADC Start Transfer.

ADEN : *ADC Converter Enable*

ADEN=0 , ADC Converter Disable.

ADEN=1 , ADC Converter Enable.

ACHEN : *ADC Converter Channel Enable*

ACHEN=0 , ADC Converter Channel Disable.

ACHEN=1 , ADC Converter Channel Enable.

CHS3~CHS0 : *ADC Channel Selection*

CHS3~CHS0 = Channel 15~0.

◆ **ADLSB**(0X141) : ***A/D Digital Data LSB 2bits of 10bits***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADLSB	AD01	AD00	-	-	-	-	-	-
R/W	R/W	R/W	-	-	-	-	-	-
RESET	0	0	-	-	-	-	-	-

AD09~AD02 : ***ADC Transfer to Digital Data bit9~bit0***

◆ **ADMSB**(0X142) : ***A/D Digital Data MSB 8bits of 10bits***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADMSB	AD09	AD08	AD07	AD06	AD05	AD04	AD03	AD02
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

AD09~AD02 : ***ADC Transfer to Digital Data bit9~bit0***

◆ **ADCON2**(0X143) : ***A/D Control Register #2***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADCON2	SHE	VREFS	-	-	-	ADCS2	ADCS1	ADCS0
R/W	R/W	R/W	-	-	-	R/W	R/W	R/W
RESET	0	0	-	-	-	0	0	0

SHE : ***ADC Sampling & Hold Enable***

SHE=0 , ADC Sampling & Hold is Enable.

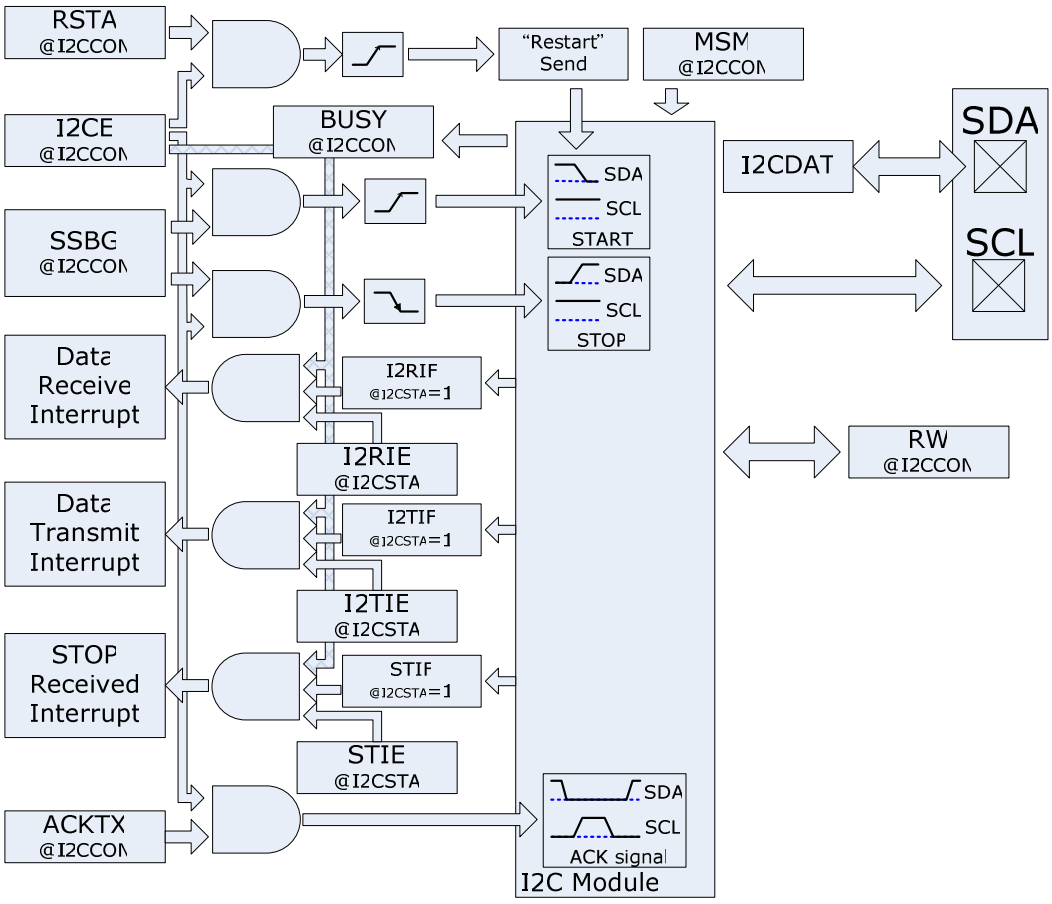
SHE=1 , ADC Sampling & Hold is Disable.

ADCS2~ADCS0 : ***ADC CLK Source:***

ADCS2	ADCS1	ADCS0	Clock (Hz)
0	0	0	Fosc/4
0	0	1	Fosc/8
0	1	0	Fosc/12
0	1	1	Fosc/16
1	0	0	Fosc/20
1	0	1	Fosc/24
1	1	0	Fosc/28
1	1	1	Fosc/32

16.0 I2C Protocol.

16.1 Overview



16.2 Registers

◆ **I2CCON**(0X144) : ***I2C Protocol control register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
I2CCON	I2CE	RSTA	SSBG	MSM	ACKTX	RW	BUSY	ARBL
R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W
RESET	0	0	0	0	0	0	0	1

I2CE : ***I2C Protocol Enable***

I2CE=0 , I2C Protocol Disable.

I2CE=1 , I2C Protocol Enable.

RSTA : ***I2C Protocol Re-Start Bit Send (Master Mode)***

RSTA=0 → 1, Generate I2C protocol "Re-Start" bit.

SSBG : ***I2C Protocol Generate Start/Stop bit (Master Mode)***

SSBG=0 → 1, Generate I2C protocol "Start" bit.

SSBG=1 → 0, Generate I2C protocol "Stop" bit.

MSM : ***I2C Protocol Master/Slave Mode***

MSM=0 , I2C Protocol Slave Mode.

MSM=1 , I2C Protocol Master Mode.

ACKTX : ***I2C ACK signal sending***

When level changed, an ACK signal will be sent to SDA by clock pulse on SCL.

RW : ***I2C Protocol RW bit in header byte***

RW=0 , Transmitter on Master, Receiver on Slave.

RW=1 , Transmitter on Slave, Receiver on Master.

BUSY : ***I2C bus status***

The bit will be set to 1 if "START" signal being detected, and clear to 0 if "STOP" signal being detected.

ARBL : ***I2C arbitration lost***

The bit will be set to 1 if the bus arbitration is lost , and cleared by software.

◆ **I2CSTA**(0X145) : ***I2C Protocol status register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
I2CSTA	I2RIE	I2RIF	I2TIE	I2TIF	STIE	STIF	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
RESET	0	0	0	0	0	0	-	-

I2RIE : ***I2C Protocol Receive Interrupt enable bit***

I2RIE=0 , I2C Protocol receive interrupt disable.

I2RIE=1 , I2C Protocol receive interrupt enable.

I2RIF : ***I2C Protocol Byte Receive Flag***

I2RIF=0 , Clear by software.

I2RIF=1 , I2C Protocol had received a byte data.

I2TIE : ***I2C Protocol Transmit Interrupt enable bit***

I2TIE=0 , I2C Protocol transmit interrupt disable.

I2TIE=1 , I2C Protocol transmit interrupt enable.

I2TIF : ***I2C Protocol Byte Transmitted Flag***

I2RIF=0 , Clear by software.

I2RIF=1 , I2C Protocol had transmitted a byte data and received the ACK/nACK signal.

STIE : ***I2C Protocol Stop Bit Received Interrupt enable bit***

STIE=0 , I2C Protocol stop bit received interrupt disable.

STIE=1 , I2C Protocol stop bit received interrupt enable.

STIF : ***I2C Protocol Stop Bit Receive Flag***

STIF=0 , Clear by software.

STIF=1 , I2C Protocol had received a “STOP” bit signal.

◆ **I2CDAT**(0X146) : ***I2C Protocol Data Store register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
I2CDAT	I2CD7	I2CD6	I2CD5	I2CD4	I2CD3	I2CD2	I2CD1	I2CD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

I2CDAT register is the buffer to store the transmit/received data.

◆ **I2CSAD**(0X147) : ***I2C Slave Address Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
I2CSAD	I2CA6	I2CA5	I2CA4	I2CA3	I2CA2	I2CA1	I2CA0	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
RESET	0	0	0	0	0	0	0	-

I2CA6~0 : *I2C Protocol address (Slave Mode)*

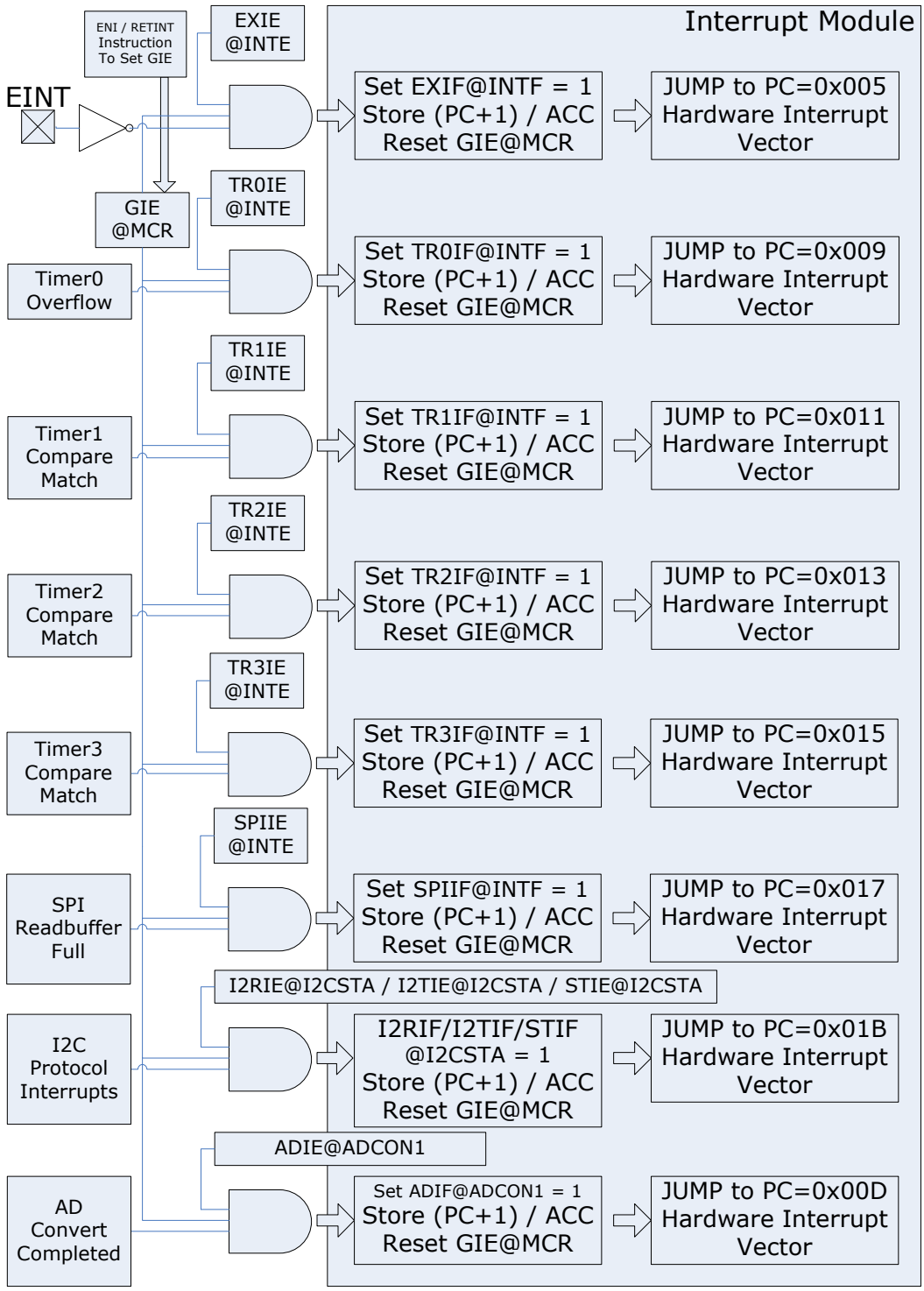
I2CA6~0 : *I2C Protocol SCL clock rate seed(Master Mode)*

SCL Clock Rate = Fosc / (I2CA + 3) x 2

Notes: I2CA cannot be zero while as clock rate seed.

17.0 Interrupts.

17.1 Overview



17.2 Registers

◆ **MCR** (0x122) : ***Main Control Register for Read / Write***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MCR	T0CS1	GIE	T0CS0	TM0CE	PAB	PS2	PS1	PS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET								

GIE : ***Global Interrupt Enable.***

GIE=0 Disable all interrupts. Execute DISI Instruction or accept Interrupt then GIE will be set to '0'. Reject any other Interrupt.

GIE=1 Global Enable all the Interrupt (Enable or not depend on others Register Enable Bit.
Execute ENI or RETI will be set to '1'. then accept others Interrupt.

◆ **INTE** (0x12F) : ***Hardware Interrupt Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTE	WDTIE	-	-	ICIE	TR1IE	SPIIE	EXIE	TR0IE
R/W	R/W	-	-	R/W	R/W	R/W	R/W	R/W
RESET	0	-	-	0	0	0	0	0

TR0IE : ***Timer 0 Interrupt Enable***

TR0IE=0 , Timer 0 Interrupt Disable .

TR0IE=1 , Timer 0 Interrupt Enable .

EXIE : ***External Interrupt Enable***

EXIE=0 , External Interrupt Disable .

EXIE=1 , External Interrupt Enable .

SPIIE : ***SPI Interrupt Enable***

SPIIE=0 , SPI Interrupt Disable .

SPIIE=1 , SPI Interrupt Enable .

TR1IE : ***Timer 1 Interrupt Enable***

TR1IE=0 , Timer 1 Interrupt Disable .

TR1IE=1 , Timer 1 Interrupt Enable .

ICIE : ***I/O port Change Interrupt Enable***

ICIE=0 , I/O Port-Change Interrupt Disable .

ICIE=1 , I/O Port-Change Interrupt Enable .

WDTIE : ***Watch Dog Timer Time-Out Interrupt Enable***

WDTIE=0 , WDT Time-Out Interrupt Disable .

WDTIE=1 , WDT Time-Out Interrupt Enable .

◆ **INTF** (0x17F) : ***Interrupt Flag Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTF	WDTIF	-	-	ICIF	TR1IF	SPIIF	EXIF	TR0IF
R/W	R/W	-	-	R/W	R/W	R/W	R/W	R/W
RESET	0	-	-	0	0	0	0	0

WDTIF : Watchdog timer overflow flag.

WDTIF = 0 , Clear it by Software.

WDTIF = 1 , If Watchdog timer overflow , this flag will be set to '1'.

ICIF : Port Change Interrupt flag.

ICIF = 0 , Clear it by Software.

ICIF = 1 , If port change interrupted , this flag will be set to '1'.

TR1IF : Timer 1 overflow flag.

TR1IF = 0 , Clear it by Software.

TR1IF = 1 , When Timer 1 overflow , this flag will be set to '1'.

SPIIF : SPI interrupt flag.

SPIIF = 0 , Clear it by Software.

SPIIF = 1 , Will be set when SPI interface interrupt occurred.

EXTIF : External interrupt flag.

EXTIF = 0 , Clear it by Software.

EXTIF = 1 , Will be set when the external interrupt occurred.

TR0IF : Timer 0 overflow flag.

TR0IF = 0 , Clear it by Software.

TR0IF = 1 , When Timer 0 overflow , this flag will be set to '1'.

17.3 Instructions

ENI	*Enable Interrupt*
Operation	MCR/GIE Flag=0
Instruction Cycle	2
Affected Flag	None
Description	Enable Interrupt
Example	DISI

DISI	*Disable Interrupt*
Operation	MCR/GIE Flag=1
Instruction Cycle	2
Affected Flag	None
Description	Disable Interrupt
Example	DISI

RETINT	***Return from Interrupt.***
Operation	(Top Stack)--> PC, MCR/GIE Flag=1
Instruction Cycle	4
Affected Flag	None
Description	Return from Interrupt ; POP The Address from Top Stack
Example	ORG 0001H JMP SF_INT NOP SF_INT: NOP **RETINT** ; Feedback to LAB1 Main: NOP INT ; Software Interrupt ; go to 0001H Addr. LAB1 NOP ; ; Push LAB1 to Top Stack

18.0 Electrical Characteristics.

18.1 DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VOP	Operating Voltage					V
IOP	Operating current					mA
ISB	Standby current					uA
FXTL	XTAL frequency					MHz
FIRC	Internal RC Frequency					MHz
IIH	Internal Pull-Low current					uA
IIL	Internal Pull-High current					uA
IOH	Output High current					mA
IOL	Output low current					mA

Appendix.1 Package Information.

Appendix.2 Programming Information.

A2.1 Programming Pins

Name	Write Pin	Writer-48	Writer-20	Notes
PB5	CS	13	19	
PB0	DIO1	38	2	
PB1	DIO2	39	3	
PB4	SCK	12	18	
-	RST	11	4	
VDD	VDD	14	20	
VSS	VSS	11	4	
PB3	VPP	37	1	

Notes.

Writer-48 : The DIP48 slot on the writer.

Writer-20 : The Wide-20 pins slot on the writer.

Appendix.3 Support Information.

A If you need any support or suggestions, there are support method which you can contact with:

E-Mail :
mcu.support@ystek.com.tw
Telephone :
+886-3-5739389(Taiwan) call for MCU.FAE Support.
Websites :
http://www.ystek.com.tw